

Novel Topology of a Common-Ground Nine-Level Double-Boost Inverter Based on Switched Capacitors

  
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Article Info	ABSTRACT
Article type: Research Article Article history: Received: ***** Received in revised form: ***** Accepted: ***** Published online: ***** Keywords: Photovoltaic (PV), Multilevel Inverter, Switched-Capacitor Inverter, Common-Ground Inverter.	There remains a vital need for inverter architectures that simultaneously offer high voltage gain, multilevel output capability, structural simplicity, and operational safety for renewable energy applications. A new single-input nine-level double-boost switched-capacitor-based inverter is proposed to address these requirements. By employing a unique switched-capacitor configuration, the proposed topology achieves a voltage gain of 2, corresponding to a maximum output voltage of $2V_{in}$ using only a single DC source, while its common-ground structure which could suppresses leakage current and reduces common-mode voltage without requiring complex control algorithms. The inverter generates a nine-level output voltage using a reduced number of power switches, while providing favorable harmonic performance. A comprehensive operational analysis is presented. To verify the proposed operating principles, detailed simulation studies are carried out in PSCAD/EMTDC. The results confirm proper multilevel operation and voltage-boosting capability, with an overall theoretical efficiency of approximately 96.74%. Finally, a comparative evaluation with recently reported inverter topologies is performed. The results indicate that the proposed inverter offers competitive performance in terms of voltage gain, component count, efficiency, and cost factor, making it a promising solution for renewable energy conversion systems.

I. Introduction

A crucial technological advancement has placed power electronics at the center of the global transition toward sustainable energy. The need for efficient, reliable, and compact power conversion systems has never been greater as the reliance on renewable energy sources, such as solar photovoltaics, continues to grow. Multilevel inverters (MLIs), which are renowned for their ability to generate high-quality output voltages with reduced harmonic distortion, play an essential role in this transition. However, as the performance requirements of these systems continue to increase, a trade-off between circuit complexity and performance remains a significant challenge [1].

Conventional multilevel topologies often suffer from increased structural complexity. To achieve a higher number of voltage levels, researchers typically employ a larger number of power switches, isolated DC sources, and gate-

driver circuits. This not only increases the cost and physical size of the system but also raises reliability concerns. In addition, many existing high-level inverters suffer from leakage-current and common-mode-voltage (CMV) issues [2], which can compromise system reliability and introduce safety concerns in grid-connected applications. Owing to their inherent voltage-boosting capability and reduced component count, switched-capacitor (SC) inverters have emerged as a promising solution. However, many existing designs still require multiple input sources or lack a common ground between the DC input and AC output, which is an important feature for reducing leakage current [3].

To avoid the requirement for bulky and costly battery storage, solar photovoltaic (PV) systems are commonly operated in grid-connected configurations. Power electronic converters play a crucial role in integrating renewable energy sources, including fuel cells and photovoltaic (PV) arrays, into such microgrids. To increase their power-handling

capability, multiple converter outputs may need to be connected in series or parallel [4], [5]. However, synchronizing the phase and amplitude of different inverter output voltages typically requires a complex control process [6]. Furthermore, an interface line impedance (Z_L) is required to connect the output voltages of these inverters to high-frequency (HF) AC grid buses. Such (Z_L) values are typically designed to be small to reduce the overall size of the conversion system. Therefore, the fundamental-frequency components of the output voltages of these HF inverters must be sufficiently high to match the peak voltage magnitude of the HF AC microgrids [7].

Particularly in photovoltaic (PV) applications, transformerless inverters are becoming increasingly important in renewable energy systems. They are designed to operate with a wide range of distributed generation (DG) technologies in both commercial and residential environments. Compared with conventional transformer-based configurations, these systems offer several advantages, including higher efficiency, higher power density, and lower cost. Moreover, eliminating the transformer from the inverter output facilitates compliance with various grid-code requirements applicable to distributed generation systems [8], [9].

Owing to their clear advantages over conventional two-level inverters, MLIs have emerged as a preferred converter technology for medium- and high-power applications [10], [11]. By employing commercially available switches with limited voltage ratings, MLIs can handle higher voltages at lower switching frequencies, resulting in reduced common-mode voltage, lower (dv/dt) stresses, and high system efficiency [12]. MLIs are also considered attractive for low-voltage and low-power applications because they can overcome several drawbacks of two-level inverters, including high switching losses, high filtering requirements, and electromagnetic emissions [13]. In principle, increasing the number of voltage levels improves the harmonic spectrum, reduces the required filter size, and lowers the common-mode voltage. Conversely, a higher number of voltage levels generally requires more active and passive components, which can increase circuit complexity and make practical implementation more challenging.

References [14] and [15] have recently introduced several reduced-switch nine-level inverter architectures. Compared with conventional multilevel inverter (MLI) topologies, these architectures achieve a comparable number of output voltage levels with fewer power semiconductor devices. Nevertheless, these topologies may have limited voltage-boosting capability, which can restrict their applicability in systems requiring increased input voltage. According to [15] and [16], some topologies require multiple isolated DC sources, and the number of required sources generally increases with the number of voltage levels. Several recently

proposed structures based on the switched-capacitor (SC) concept are presented in [17] and [18]. In these topologies, each capacitor is alternately connected to the DC source in parallel and in series during different operating states. This configuration enables the capacitors to be charged in parallel and subsequently discharged in series to increase the output voltage. Although topologies capable of generating nine-level output voltages are further discussed in [19], it should be noted that their voltage-boosting capability remains limited, with a maximum voltage gain of only two.

A nine-level switched-capacitor-based multilevel inverter with quadruple voltage-boosting capability is reported in [20]. The topology is intended for PV applications and is suitable for transformerless grid integration. A hybrid T-type nine-level inverter with threefold voltage-boosting capability for PV applications is presented in [21]. It employs a five-level T-type module at the output and four capacitors for voltage boosting. A reduced-switch quadruple-boost nine-level inverter for electric vehicle (EV) and motor-drive applications is described in [22].

Based on the widely used five-level active-neutral-point-clamped (5L-ANPC) structure, [23] proposes a hybrid nine-level inverter for high-efficiency applications. The proposed inverter eliminates the need for higher-voltage-rated switches while reducing the number of active and passive components compared with conventional ANPC-based topologies. The single-phase switched-capacitor-based MLI proposed in [24] can generate a 13-level AC output voltage with voltage gains of three and six. The same structure can also produce a single-phase nine-level AC output voltage with a voltage gain of four. These voltage levels and gains can be achieved simply by changing the switching strategy used to control the switches, without modifying the proposed SC-MLI structure [24].

A reduced-component switched-capacitor boost multilevel inverter is presented in [25]. The converter requires only two capacitors and eight switches to generate a nine-level stepped-up output voltage. Phase-disposition pulse-width modulation (PD-PWM) is employed to generate the required nine-level switching pattern.

Also, in [26], a new basic unit for multilevel inverter is presented. A cascaded connection of the presented topology is recommended. To determine the magnitude of dc voltage sources, a new algorithm is presented. For the suggested algorithm, different performance parameters such as total voltage rating of switches (TVRS), number of gate drivers, and number of required sources are calculated as a function of the number of output voltage levels and are compared with other topologies, in which the number of power electronic components and rating voltage across the switches are lower.

There remains a need for an inverter architecture that provides a high number of output voltage levels while maintaining structural simplicity and operational safety. This

paper introduces a novel single-input, common-ground, nine-level switched-capacitor-based inverter designed to bridge this gap. By utilizing a unique SC configuration, the proposed topology achieves a significant voltage gain using only one DC source, while the common-ground feature which could suppresses leakage current without the need for complex control algorithms. Throughout this study, we provide a comprehensive analysis of the circuit's operation, its self-balancing capacitor voltage characteristics, and a comparative evaluation against state-of-the-art topologies. Our objective is to present a solution that is not only mathematically robust but also practically viable for the next generation of compact, high-efficiency energy conversion systems.

To address the aforementioned challenges in PV applications, this paper introduces a novel common-ground nine-level switched-capacitor-based inverter with the following key features:

- Uses a single DC input source
- Achieves a twofold voltage gain
- Reduces the voltage stress across selected switches
- Operates two of the nine switches at the fundamental frequency
- Requires only one switching transition per cycle for one switch and one diode
- Provides a common ground between the input source and the load
- Requires fewer power switches than conventional topologies

The remainder of this paper is organized as follows: Section II provides a detailed description of the proposed nine-level topology and its operating modes. Section III presents the loss analysis and capacitor design considerations. Section IV presents the simulation results of the proposed topology. A comparative analysis with recently developed nine-level topologies is provided in Section V. Finally, the conclusions are presented in Section VI.

II. Nine-Level Switched-Capacitor- Inverter

A. Topology Description

In this section, the proposed common-ground nine-level switched-capacitor-based inverter is presented and analyzed. Fig. 1 illustrates the proposed topology, which is based on a multilevel inverter (MLI) configuration. As shown in the figure, the topology comprises nine power switches (S1–S9), two power diodes (D1 and D2), and three capacitors (C1, C2, and C3). By utilizing the appropriate switching states and capacitor configurations, a nine-level output voltage waveform is generated.

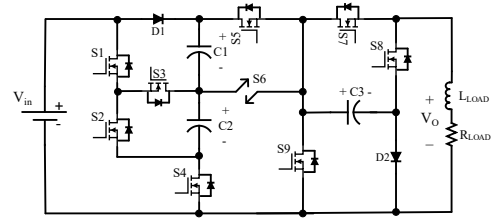


Fig. 1. Nine-level common ground switched-capacitor inverter.

The switching states of the proposed topology are listed in Table I, where the green color indicates the main switching states during the positive and negative half-cycles, while the red color represents the auxiliary switching states. For the capacitors, the charging, discharging, and no-change states are indicated by the letters “C,” “D,” and “F,” respectively, as listed in Table II.

TABLE I Switching states of the proposed nine-level inverter

Output Level	S1	S2	S3	S4	S5	S6	S7	S8	S9	D1	D2
0 ⁺	0	0	0	1	0	0	1	0	1	1	0
+V _{in} /2	0	0	0	1	0	1	1	0	0	1	0
+V _{in}	0	0	0	1	0	1	1	0	0	1	0
+3V _{in} /2	1	0	0	0	1	0	1	0	0	0	0
+2V _{in}	1	1	0	0	1	0	1	0	0	0	1
0 ⁻	1	1	0	0	1	0	0	1	0	0	1
-V _{in} /2	1	0	1	0	1	0	0	1	0	0	0
-V _{in}	0	0	0	1	1	0	0	1	0	1	0
-3V _{in} /2	0	0	0	1	0	1	0	1	0	1	0
-2V _{in}	0	0	0	1	0	0	0	1	1	1	0

TABLE II Capacitor charging and discharging states of the proposed nine-level inverter

Capacitor	0 ⁺	+V _{in} /2	+V _{in}	+3V _{in} /2	+2V _{in}	0 ⁻	-V _{in} /2	-V _{in}	-3V _{in} /2	-2V _{in}
C1	C	C	C	D	D	D	C	C	C	C
C2	C	D	C	F	D	D	F	C	C	C
C3	F	F	F	F	C	C	D	D	D	D

B. Operating Modes of the Proposed Nine-Level Inverter

The operating principles of the proposed nine-level inverter are described in this section. The inverter is capable of generating nine voltage levels, namely 0, $\pm V_{in}/2$, $\pm V_{in}$, $\pm 3V_{in}/2$, and $\pm 2V_{in}$. All operating modes are shown in Fig. 2.

a) Zero-Voltage Level

The zero-voltage state, shown in Fig. 2(a) and Fig. 2(f), is established by turning on switches S7 and S9 during positive load current flow or switch S8 together with diode D2 during negative current flow. During the positive half-cycle, capacitors C1 and C2 are charged to $V_{in}/2$ through switch S4 and diode D1. During the negative half-cycle, capacitor C3 is charged to $2V_{in}$ via switches S1, S2, and S5 and diode D2. Meanwhile, depending on the load-current direction, capacitors C1 and C2 may discharge and release their stored energy.

$$\begin{aligned} V_{C1} + V_{C2} &= V_{in} && \text{for positive flow} && (1) \\ V_{C3} &= V_{in} + V_{C1} + V_{C2} && \text{for negative flow} && (2) \end{aligned}$$

b) $+V_{in}/2$ Voltage Level

As shown in Fig. 2(b), capacitor C1 is charged through switch S4 and diode D1, while capacitor C2 supplies the load through switches S4, S6, and S7, generating an output voltage of $+V_{in}/2$.

$$V_o = V_{C2} \quad (3)$$

c) $+V_{in}$ Voltage Level

Fig. 2(c) depicts the operating mode corresponding to $+V_{in}$. In this state, capacitors C1 and C2 are charged through switch S4 and diode D1, while the load is supplied directly by the input source through switches S5 and S7 and diode D1.

$$V_o = V_{in} \quad (4)$$

d) $+3V_{in}/2$ Voltage Level

The $+3V_{in}/2$ voltage level shown in Fig. 2(d) is generated through switches S1, S3, S5, and S7. In this operating mode, the input source and capacitor C1 are connected in series to supply the load, while capacitor C1 is simultaneously maintained at its desired voltage level.

$$V_o = V_{in} + V_{C1} \quad (5)$$

e) $+2V_{in}$ Voltage Level

As shown in Fig. 2(e), the maximum positive output voltage of $+2V_{in}$ is obtained through switches S1, S2, S5, and S7. During this interval, capacitors C1 and C2 are discharged, whereas capacitor C3 is recharged through switches S1, S2, S5, and diode D2.

$$V_o = V_{in} + V_{C1} + V_{C2} \quad (6)$$

f) $-V_{in}/2$ Voltage Level

For the $-V_{in}/2$ level depicted in Fig. 2(g), capacitor C3 discharges to the capacitor C1 and the input through switches S1, S3, S5, and S8 to supply the load.

$$V_o = V_{in} + V_{C1} - V_{C3} \quad (7)$$

g) $-V_{in}$ Voltage Level

The operating mode associated with $-V_{in}$ is illustrated in Fig. 2(h). Capacitors C1 and C2 are charged through switch S4 and diode D1, while capacitor C3 supplies the load through diode D1 and switches S5 and S8 and V_{in} . Consequently, capacitor C3 is discharged during this interval.

$$V_o = V_{in} - V_{C3} \quad (8)$$

h) $-3V_{in}/2$ Voltage Level

As shown in Fig. 2(i), the $-3V_{in}/2$ voltage level is generated by the series combination of capacitor C3 and capacitor C2 through switches S4, S6, and S8. At the same time, capacitor C1 is charged to $V_{in}/2$ through switch S4 and diode D1.

$$V_o = V_{C2} - V_{C3} \quad (9)$$

i) $-2V_{in}$ Voltage Level

The maximum negative output voltage, $-2V_{in}$, is obtained as illustrated in Fig. 2(j). In this mode, capacitor C3 supplies the load through switches S8 and S9, generating the required voltage level. Meanwhile, capacitors C1 and C2 are charged to $V_{in}/2$ through switch S4 and diode D1.

$$V_o = -V_{C3} \quad (10)$$

III. Design considerations of the proposed nine-level inverter

A. Capacitor Design Considerations

To determine the capacitance values of the proposed topology, the longest capacitor discharge interval is considered. The capacitor C1 discharges from the $+3V_{in}/2$ to the $0+$ voltage level, capacitor C2 discharges at $+V_{in}/2$ and $+2V_{in}$, and capacitor C3 discharges from $-V_{in}/2$ to $-2V_{in}$. The highest amount of discharge in each half cycle can be calculated as follows [25]:

$$Q_{Ci} = \int_{t_b}^{t_a} I_{load} \sin(2\pi f_m t) dt \quad (11)$$

where Q_{Ci} is the maximum discharge amount of the capacitor, t_a and t_b is the start and end timings of discharge period shown in Fig. 3. The capacitor value could be calculated as:

$$C_i > \frac{Q_{Ci}}{kV_C} \quad (12)$$

where k represents the capacitor voltage ripple in per unit (p.u.). Fig. 3 illustrates the output voltage waveform and its corresponding time intervals during the positive half-cycle, which are utilized in the capacitor design calculations.

The capacitance values of the switched capacitors are determined based on the allowable voltage ripple and the operating intervals of each capacitor. For capacitors C1, C2, and C3, the effective discharge durations are 1.875–8.125 ms, 2.84–7.16 ms, and 10–20 ms, respectively. Considering a load current of 2 A, a fundamental frequency of 50 Hz, and a permissible voltage ripple coefficient of 1.5% for capacitors C1 and C2, and 0.5% for capacitor C3, the capacitor voltages are selected as $V_{C1} = 100$ V, $V_{C2} = 100$ V, and $V_{C3} = 400$ V. Based on these design specifications, the required capacitance values are obtained as 7066 μ F for C1, 5333 μ F for C2, and 6350 μ F for C3.

It should be noted that, similar to other switched-capacitor multilevel inverters, the proposed topology is primarily intended for low- and medium-power applications. As the output power increases, the capacitor discharge current also increases, which may lead to larger capacitor voltage ripple

and consequently higher output voltage distortion if the capacitance values are not properly designed. Therefore, the capacitor values in this work are selected based on the

maximum discharge intervals and a permissible voltage ripple mentioned above, ensuring stable capacitor voltages under the rated operating conditions.

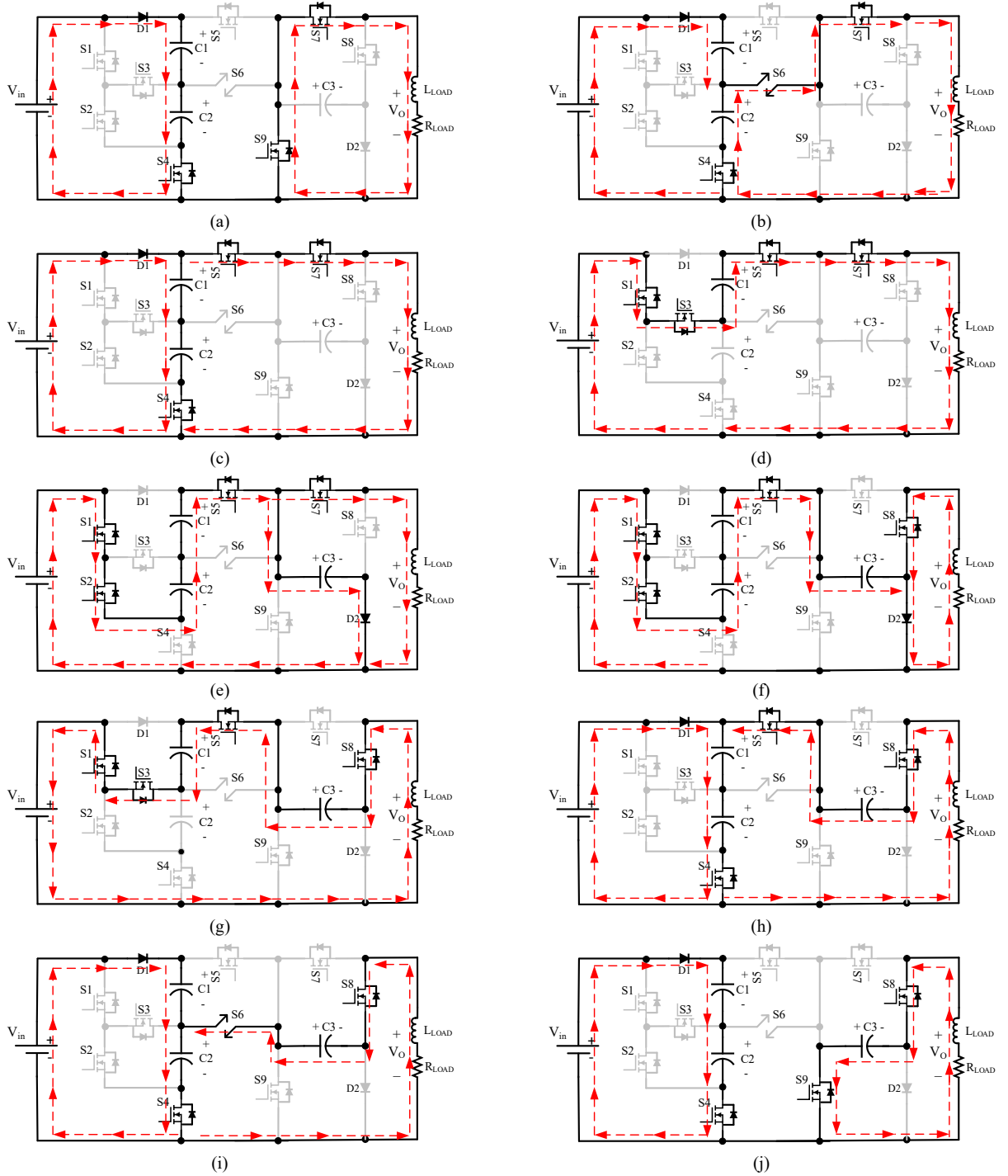


Fig. 2. Operating modes of the proposed nine-level inverter. (a) zero state (positive flow), (b) $+V_{in}/2$, (c) $+V_{in}$, (d) $+3V_{in}/2$, (e) $+2V_{in}$, (f) zero state (negative flow), (g) $-V_{in}/2$, (h) $-V_{in}$, (i) $-3V_{in}/2$, (j) $-2V_{in}$ state.

Although the calculated capacitance values provide the required voltage-ripple performance, their practical implementation should also be considered. The selected values at the specified voltage ratings may result in relatively large electrolytic capacitors and therefore contribute to the overall volume, weight, and cost of the converter.

In a practical implementation, the capacitors should be selected with sufficient ripple-current capability, appropriate ESR, and adequate lifetime under the expected operating temperature and electrical stress. In addition, the relatively high stored energy requires an appropriate pre-charging or

current-limiting circuit to restrict the inrush current during converter start-up.

It should therefore be noted that the compactness of the proposed topology is mainly associated with its reduced number of semiconductor and passive components compared with the considered topologies, rather than the complete elimination of the volume associated with energy-storage capacitors. The selected capacitance values represent a trade-off between capacitor-voltage ripple and practical capacitor size. Further optimization using higher-energy-density capacitor technologies or optimized capacitance values may reduce the physical volume and improve the overall power density in future implementations.

It should be noted that the proposed topology does not employ an additional soft-charging cell for limiting the capacitor charging current. Therefore, the initial charging transient and the associated peak current should be considered in the practical implementation of the converter. Appropriate pre-charging circuitry and suitable current ratings for the semiconductor devices and capacitors can be employed to limit the inrush current and ensure reliable operation. Dedicated soft-charging cells, as reported in [27]–[29], can further mitigate the charging-current stress; however, their integration would increase the component count and circuit complexity. The incorporation of an optimized soft-charging mechanism is therefore considered a potential direction for future development.

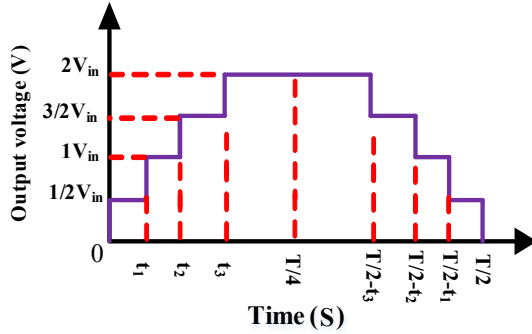


Fig. 3. The output voltage levels and their corresponding time intervals during the positive half-cycle.

B. Power Loss and Efficiency Analysis

To assess the performance of the proposed nine-level switched-capacitor inverter, a comprehensive power-loss analysis is carried out. The total power dissipation consists of three major components: semiconductor switching losses, conduction losses, and capacitor losses.

The switching losses occur during the turn-on and turn-off transitions of the semiconductor devices. The energy dissipated during each switching event depends on the instantaneous current and voltage waveforms across the device during the commutation interval. Accordingly, the turn-on and turn-off losses of the i th switch are calculated using (13) and (14), respectively. Since each semiconductor

undergoes multiple switching transitions within a fundamental cycle, the number of turn-on and turn-off operations is determined by (15), which relates the carrier frequency to the modulation frequency. By summing the switching losses of all active switches, the total switching loss of the inverter can be obtained from (16).

In addition to switching losses, conduction losses occur due to the non-zero on-state voltage drop and conduction resistance of the semiconductor devices. Based on the equivalent circuits, the conduction losses of the power switches and diodes are evaluated using (17) and (18), respectively [30]. These equivalent circuits represent the current conduction paths corresponding to the various operating states of the inverter and provide the basis for determining the average and RMS currents flowing through each device.

The switched capacitors also contribute to the overall power dissipation. The capacitor losses consist of ESR-related conduction losses and voltage-ripple losses. The ESR losses are determined from the RMS current flowing through each capacitor, as expressed in (19), while the losses associated with capacitor voltage ripple are calculated using (20). These losses are particularly important in switched-capacitor topologies because of the continuous charging and discharging processes [30].

The overall power loss of the proposed inverter is obtained by summing all semiconductor and capacitor loss components according to (21). Subsequently, the overall conversion efficiency is calculated using (22).

$$P_{S,i(ON)} = f_s \int_0^{t_{ON}} V_{Sw,i}(t) i_{Sw,i}(t) dt \quad (13)$$

$$= \frac{1}{6} \times f_s \times V_{Sw,i} \times i_{Sw,i}$$

$$P_{S,i(OFF)} = f_s \int_0^{t_{OFF}} V_{Sw,i}(t) i_{Sw,i}(t) dt \quad (14)$$

$$= \frac{1}{6} \times f_s \times V_{Sw,i} \times i_{Sw,i}$$

$$N_{s,on} = N_{s,off} = \frac{f_{cr}}{f_m} \quad (15)$$

$$P_{SL(Total)} = \sum_{j=1}^{N_{SW}} \left(\sum_{i=1}^{N_{on(i)}} P_{SL-on(ij)} + \sum_{i=1}^{N_{off(i)}} P_{SL-off(ij)} \right) \quad (16)$$

$$P_{SW-con} = V_{Sw-on} \times i_{Sw-avg} + R_{DS-on} \times i_{Sw-rms}^2 \quad (17)$$

$$P_{D-con} = V_{D-on} \times i_{D-avg} + R_{D-on} \times i_{D-rms}^2 \quad (18)$$

$$P_{C-con} = \sum_{i=1}^n R_{C-i} \times i_{Crms-i}^2 \quad (19)$$

$$P_{C,ripple} = \frac{f_l}{2} (C_1 \Delta V_{C1}^2 + C_2 \Delta V_{C2}^2 + C_3 \Delta V_{C3}^2) \quad (20)$$

$$P_{losses} = P_{SW-con(Total)} + P_{SL(Total)} \quad (21)$$

$$\eta = \left(\frac{P_{in} - P_{losses}}{P_{in}} \right) \times 100 \quad (22)$$

In above relations, $P_{S,i(ON)}$ and $P_{S,i(OFF)}$ are the turn-on and turn-off switching losses of the i th switch, respectively., and $N_{S,off}$ and $N_{S,on}$ denote the numbers of turn-off and turn-on events in one cycle, respectively. f_m is the modulating frequency and f_{cr} is the carrier frequency.

Based on the analytical calculations, the switching losses of the active semiconductor devices are 7.038 mW, whereas their conduction losses are 5.792 W. The total losses associated with the switched capacitors are found to be 7.237 W. Consequently, the overall power loss of the proposed inverter is 13.036 W. Considering an input power of 400 W, the output power is approximately 386.96 W, resulting in an overall analytical and theoretical estimated value efficiency of 96.74%. These results demonstrate the effectiveness of the proposed topology in achieving high-efficiency power

conversion while maintaining a reduced component count and enhanced output-voltage gain.

C. Voltage Stresses of Power Semiconductors

In the proposed topology, four switches (S1, S2, S3, and S6) withstand a blocking voltage of $(V_{in}/2)$. Two switches (S4 and S5) and diode D1 experience a blocking voltage of (V_{in}) , whereas three switches (S7-S9) and diode D2 withstand a voltage of $(2V_{in})$. The total standing voltage ($TSV_{p.u.}$) of the single-source inverter can be expressed as given in (23).

$$TSV_{p.u.} = \frac{\sum V_{sw,off} + \sum V_{D,off}}{V_{omax}} \quad (23)$$

where the $V_{D,off}$ and $V_{sw,off}$ denote the diode and switch blocking voltages, respectively, and V_{omax} is the maximum output voltage. $TSV_{p.u.}$ of the suggested nine-level inverter is 6.5. Also, the maximum blocking voltage of each semiconductor is shown in Fig. 4. Fig. 5 illustrates the voltage stress of all switches and diodes considering all voltage levels at the output.

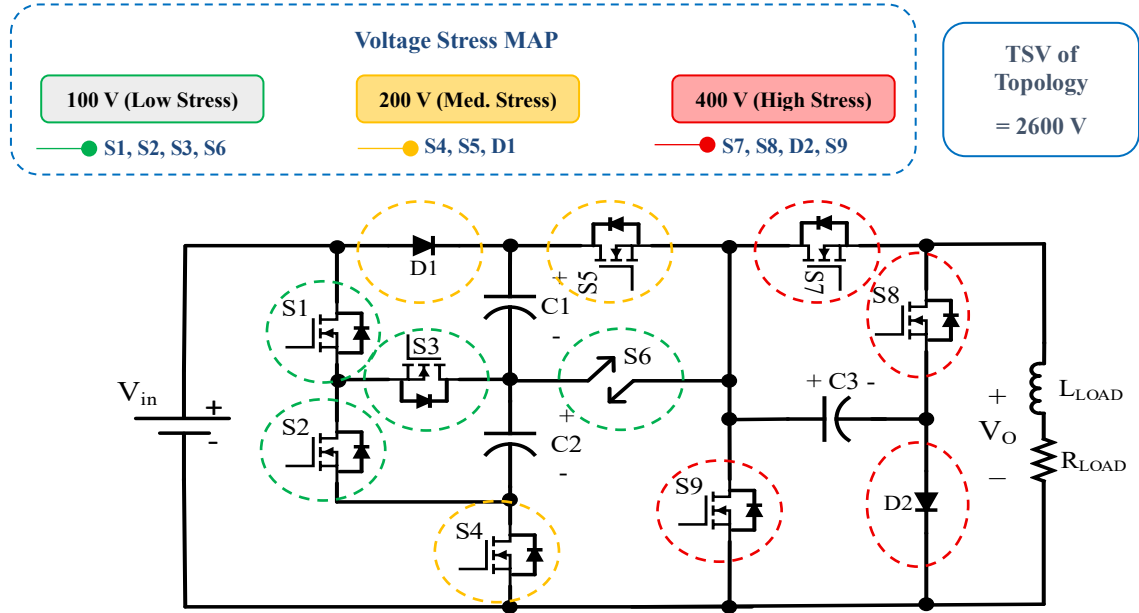


Fig. 4. Voltage stress distribution of the semiconductor devices in the proposed common-ground nine-level switched-capacitor inverter. Green, yellow, and red labels indicate low (100 V), medium (200 V), and high (400 V) blocking voltage stresses, respectively.

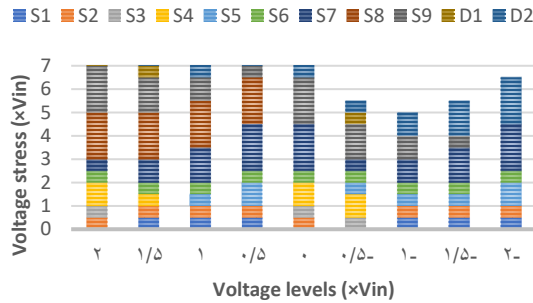


Fig. 5. Voltage stresses of power semiconductors in different voltage levels.

IV. Simulation Result

The performance of the proposed topology is verified through simulation results. The simulations are carried out using PSCAD/EMTDC software, version 4.2.1. The specifications and ratings of the components used in the proposed topology are summarized in Table III.

TABLE III Values used in the simulation results

parameters	value
Input voltage	200 V
Output Power	400 W
Carrier frequency	5 kHz
Funfamental frequency	50 Hz
C1 & C2	10000 μ F
C3	6800 μ F
R_L	200 Ω
L_L	300 mH

R_{ESR}	0.05 Ω
V_F	0.7 V
R_{on}	0.4 Ω
R_D	0.04 Ω
t_r	55 ns
t_f	100 ns
D1 and D2	MUR1560
S1-S9	IRFP460

A sinusoidal pulse-width modulation (SPWM) strategy based on natural sampling is employed to generate the gate signals. A single triangular carrier with a frequency of 5 kHz is directly compared with a sinusoidal reference waveform having a fundamental frequency of 50 Hz. The modulation index is set to 0.9. Since natural sampling is employed, the sinusoidal reference is continuously compared with the triangular carrier to determine the PWM pulses. The resulting PWM signals are then processed by the logic circuits to generate the appropriate gate signals according to the switching states listed in Table 1. In particular, two of the nine switches operate at the fundamental frequency, while one switch and one diode undergo only one switching transition per fundamental cycle.

It should be noted that the modulation index and reference waveform are kept constant in the simulations presented in this study. The transient results presented in this section are intended to demonstrate the inverter behavior under load and input-voltage variations, while the change from a predominantly resistive to an inductive load also results in a variation of the operating power factor. Since the proposed converter employs a predefined sinusoidal modulation strategy without a closed-loop PI controller, comprehensive reference-tracking analysis and controller-based dynamic regulation are beyond the scope of the present topology-focused study.

This section discusses the simulation performance of the proposed nine-level inverter using PSCAD/EMTDC software. Fig. 6(a) presents the generated output voltage waveform. The corresponding output voltage and current waveforms for a resistive load are shown in Fig. 6(b). It can be seen that the inverter produces nine voltage levels, namely 0, $\pm(V_{in}/2)$, $\pm(V_{in})$, $\pm(3V_{in}/2)$, and $\pm(2V_{in})$. Under the resistive load condition, the output current follows the voltage waveform and exhibits a stepped profile. Moreover, Fig. 6(c) demonstrates the output voltage and current characteristics under a resistive-inductive load. In this case, the current waveform becomes nearly sinusoidal and exhibits a phase lag with respect to the output voltage due to the presence of the inductive component in the load.

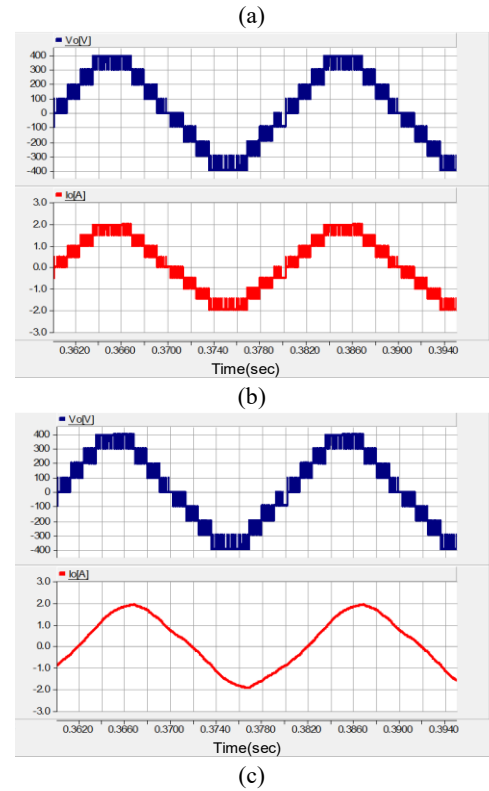
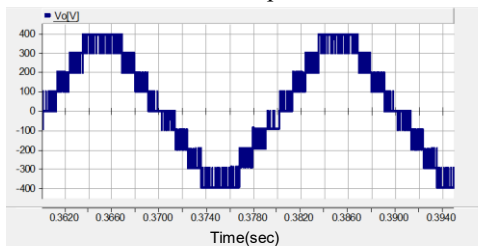


Fig. 6. Simulation waveforms of the proposed nine-level inverter: (a) output voltage, (b) output voltage and current for a resistive load, and (c) output voltage and current for a resistive-inductive load.

The voltage waveforms of capacitors C1–C3 are presented in Fig. 7. It can be seen that the voltages across capacitors C1 and C2 are maintained at approximately 100 V, whereas the voltage across capacitor C3 is regulated at around 400 V.

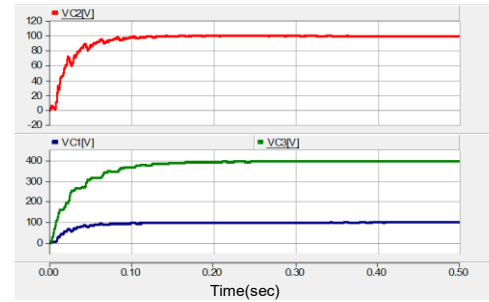


Fig. 7. Voltage waveforms of the capacitors in the proposed converter.

The voltage and current waveforms of the proposed inverter under different conditions are presented in Fig. 8. Fig. 8(a) illustrates the response to sudden load changes under a resistive load. Fig. 8(b) illustrates the transition from a resistive load to a resistive-inductive load. Fig. 8(c) illustrates the load response under a resistive-inductive load. In all circumstances, the inverter output voltage remains constant.

The voltage stresses across the power MOSFETs and diodes of the proposed nine-level inverter are illustrated in

Fig. 9. Fig. 9(a) presents the voltage stresses of switches S1 and S3, both of which are approximately 100 V. The voltage stresses of switches S2 and S4 are shown in Fig. 9(b), where S2 experiences a voltage stress of about 100 V, while S4 withstands approximately 200 V. Fig. 9(c) depicts the voltage stresses of switch S5 and diode D1, each experiencing a voltage stress of nearly 200 V. The voltage stresses of switch S7 and diode D2 are illustrated in Fig. 9(d), with both components subjected to a voltage stress of approximately 400 V. In addition, Fig. 9(e) shows the voltage stresses of switches S6 and S8, which are around 100 V and 400 V, respectively. In addition, switch S9 must withstand a voltage stress of 400 V. Therefore, among the nine switches and two diodes, four power semiconductors withstand a voltage stress of $(2V_{in})$, three switches experience a voltage stress of (V_{in}) , and the remaining four power semiconductors are subjected to a voltage stress of $(V_{in}/2)$.

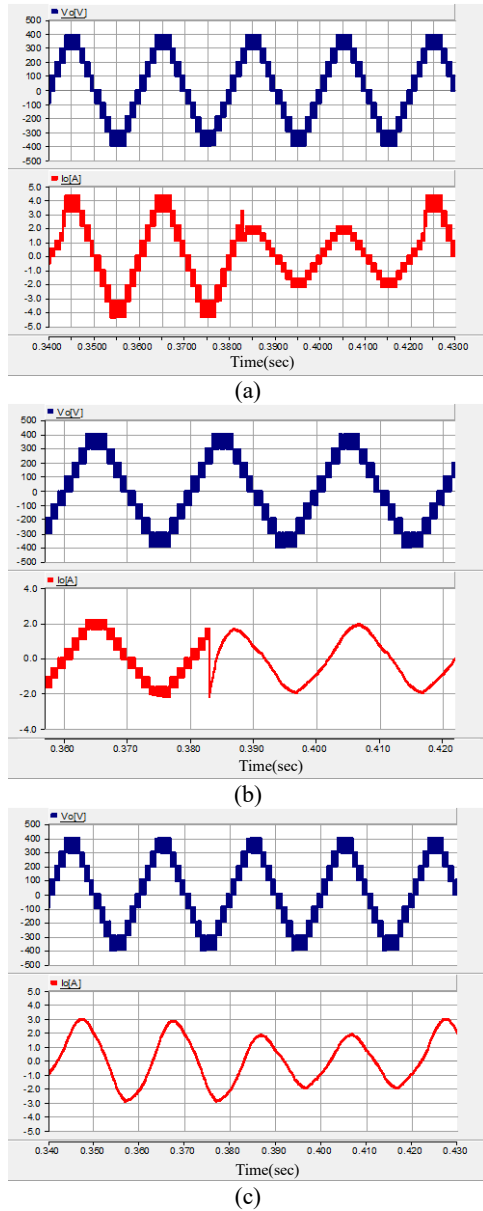
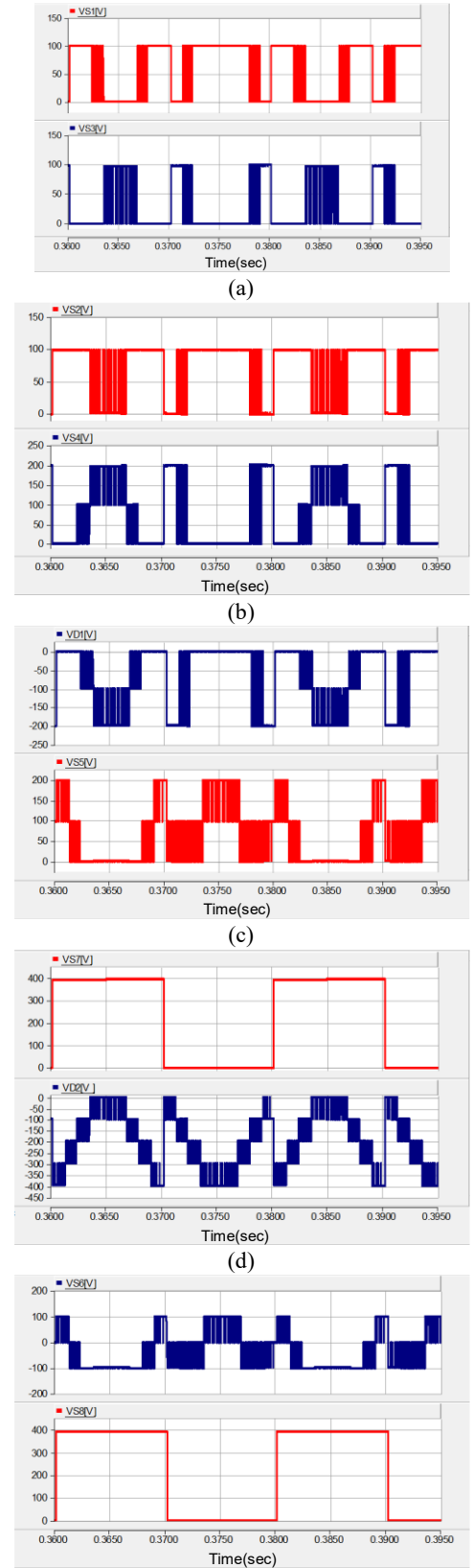


Fig. 8. Simulation results of the voltage and current of the proposed converter under different load conditions: (a) pure resistive load, (b) transition from a resistive load to a resistive-inductive load, (c) resistive-inductive load.



(e)

Fig. 9. Simulation results of the voltage stresses across the power MOSFETs and diodes of the proposed converter: (a) switches S1 and S3, (b) switches S2 and S4, (c) switch S5 and diode D1, (d) switch S7 and diode D2, and (e) switches S6 and S8.

V. Comparative Study

In this section, a comprehensive comparison between the proposed nine-level inverter and recently reported state-of-the-art topologies is presented in terms of the number of power semiconductors, passive components, gate driver circuits, DC sources, switches in the charging circuit, voltage gain, total standing voltage ($TSV_{p.u.}$), maximum blocking voltage, total conducting device (TCD), TCD_{avg} , number of

semiconductors blocking $V_{o,max}$ and cost factor (CF). The comparative results are summarized in Table IV. The cost factor is calculated using the following equation [31].

$$CF = N_{sw} + N_d + N_c + N_L + N_s + N_{dr} + \alpha TSV_{p.u.} \quad (24)$$

Where (α) is a weighting factor. If (α) is greater than one, the total standing voltage is given higher importance. If (α) is less than one, the number of switching components is considered more significant. When (α) is equal to one, both the total standing voltage and the number of switching components have equal importance. Here, α is considered 1, all topologies are compared using the same evaluation criterion.

TABLE IV Comparative Study of The Proposed Nine-Level Inverter With Related Topologies

Ref.	N_{sw}	N_d	N_c	N_s	N_{dr}	G	CG	$TSV_{p.u.}$	TCD				TCD_{avg}	No. S.C. blocking $V_{o,max}$	CF	η (%)
									$\pm 1^{st}$	$\pm 2^{nd}$	$\pm 3^{rd}$	$\pm 4^{th}$				
[32]	12	2	2	2	12	2	NO	5	5	6	4	6	5.25	4	35	95.64
[33]	10	2	2	2	10	2	YES	5	5	6	2	5	4.5	2	31	95.89
[34]	12	0	3	1	12	1	NO	5	2	3	6	4	3.75	6	33	95.73
[35]	12	0	2	1	11	2	NO	5.5	5	4	0	4	3.25	0	31.5	96.47
[36]	11	0	2	1	7	2	NO	5	5	4	0	5	3.5	0	26	96.56
[37]	11	0	3	1	10	2	NO	5	5	6	0	5	4	0	30	96.75
[38]	9	2	2	1	9	2	NO	6.5	4	5	4	4	4.25	4	29.5	96.87
[39]	12	0	3	1	11	2	NO	5.5	5	4	0	4	3.25	0	32.5	97.45
[40]	8	2	2	1	8	3	NO	6	4	4	4	0	3	4	27	95.5
[41]	7	7	3	1	7	1.5	NO	7	3	6	0	-	3	0	32	96.8
[P]	9	2	3	1	9	2	YES	6.5	4	3	4	4	3.75	4	30.5	96.74
[32]	12	2	2	2	12	2	NO	5	5	6	4	6	5.25	4	35	95.64

It should be noted that the cost factor (CF) adopted in this study follows the conventional definition widely reported in the literature for multilevel inverter comparison. The primary objective is to provide a consistent basis for comparing converter structures using the same evaluation criterion. However, this metric assumes identical weighting for different components and does not explicitly incorporate voltage gain, physical size, or power density. In particular, the proposed topology requires relatively large capacitors, which may contribute significantly to the practical cost, volume, and weight of the converter. The CF index does not directly account for the capacitance, voltage rating, ripple-current capability, ESR, or physical dimensions of these capacitors. Therefore, although CF provides a useful first-order topology-level comparison, it should not be regarded as a complete indicator of the overall implementation cost or physical size of the converter. A more realistic cost and volume assessment would require considering the specifications and prices of commercially available semiconductor devices and capacitors under comparable operating conditions.

Although the proposed topology reduces the number of semiconductor components, the required capacitor bank remains a practical limitation. Due to the relatively large capacitance values, the capacitor bank can become a dominant contributor to the converter volume, weight, and

cost. Therefore, the compactness advantage of the proposed topology should be interpreted mainly from the topology and semiconductor-count perspectives rather than as a complete hardware-volume reduction.

As can be observed from Table IV, the proposed nine-level inverter achieves the lowest number of power switches compared with the topologies reported in [32]–[41], except [40] and [41]. Although the number of diodes in the proposed topology is identical to those in [32], [33], [38], and [40], several other structures in [34]–[37], and [39] do not employ any diodes. On the contrary, [41] employs 7 diodes. The proposed inverter requires three capacitors to generate ($2V_{in}$) at the output, similar to the configurations in [37] and [39], whereas the topologies in [32], [33], [35], [36], and [38] utilize only two capacitors. In addition, the proposed structure operates with a single DC source to achieve ($2V_{in}$), while the approaches in [32] and [33] require two input sources.

The voltage gain of the proposed inverter is equal to 2, which is consistent with most of the compared topologies, except for [34], [40], and [41], where the gain is 1, 3, and 1.5, respectively. A key advantage of the proposed configuration, along with [33], is the presence of a common ground between the input and output, making it suitable for photovoltaic applications. In contrast, the remaining topologies in [32], [34]–[41] do not provide a common-

ground structure. The total voltage stress (TSV) of the suggested topology is 6.5, which is slightly better than some reported approaches but comparable to or better than those in [38], and [41]. The proposed inverter achieves a lower CF than most of the referenced topologies, except for [36]–[38] and [40].

Among the recently reported switched-capacitor multilevel inverters, the topologies presented in [37] and [39] exhibit the closest characteristics to the proposed converter, since they also employ a single DC source and provide twofold voltage boosting capability. However, their circuit configuration, capacitor charging mechanism, and current flow paths differ significantly from the proposed topology. In contrast, the proposed inverter employs a different switched-capacitor arrangement that achieves the same voltage gain with a simplified circuit structure, reduced voltage stress across several semiconductor devices, and improved component utilization while preserving the common-ground feature. Therefore, the originality of the proposed converter lies in its circuit topology and operating mechanism rather than merely in the output voltage levels or voltage gain. In contrast, the topologies in [37] and [39] do not employ a common-ground structure.

Based on the relations mentioned above, the total power loss of the proposed topology is calculated as 13.036 W. Accordingly, the theoretically estimated efficiency value of the nine-level inverter is determined to be 96.74%. The proposed nine-level inverter demonstrates higher efficiency compared with the topologies reported in [32]–[36], as summarized in Table IV, while also utilizing a reduced number of power switches and passive components. The efficiency values reported in Table 5 are provided for reference only and should not be considered an absolute ranking of the compared topologies. The reported efficiencies in the different references were obtained under different operating conditions, including semiconductor technologies, switching frequencies, load conditions, and power ratings. Therefore, a direct efficiency comparison should be interpreted with caution. Fig. 10 illustrates the distribution of power losses in the proposed topology corresponding to different loss components. Fig. 11 presents a comparison of the efficiencies of the proposed inverter with other reported topologies.

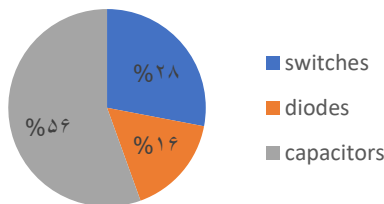


Fig. 10. Pie chart showing the distribution of theoretical power losses in the proposed topology.

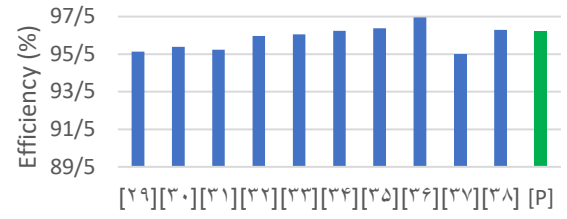


Fig. 11. Efficiency comparison of the proposed inverter with related topologies.

VI. Conclusions

This paper presents a new common-ground nine-level double-boost inverter with a single input that is suitable for photovoltaic applications. The proposed topology achieves a voltage gain of up to $2V_{in}$ using a single DC source and a switched-capacitor structure, while maintaining a common ground between the input and output. This configuration effectively mitigates common-mode and differential-mode voltages, consequently reducing leakage current and grid-side harmonic distortion. With only nine switches, the inverter offers a new structure with a reduced component count, contributing to improved efficiency and a reasonable overall cost factor. In addition, the nine-level output voltage significantly reduces harmonic distortion and allows for a smaller grid-filter inductor. Simulation results validate the theoretical analysis and demonstrate reliable operation, confirming an overall theoretical efficiency of 96.74%. These results highlight the proposed inverter as a promising candidate for low- to medium-power renewable energy systems requiring voltage-boosting capability, and enhanced power quality. Future work will focus on grid-connected implementation and the evaluation of advanced control strategies, such as model predictive control, to further improve dynamic performance and robustness under varying operating conditions.

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Appendix A



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