International Journal Of
Industrial Electronics Control and Optimization
Print ISSN: 3517-2645
Online ISSN: 3568-2645
Homepage: https://ieco.usb.ac.ir/

Improved Boost Topology According to the Voltage Lift Technique

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Article Info

Article type:
Research Article

Article history:
Received: 07-January-2025
Received in revised form: 06-May-2025
Accepted: 11-May-2025
Published online:21-March-2026

Keywords:
Boost converter,
multiplier cell,
HID lamps,
Luo .

ABSTRACT

This paper proposes a novel non-isolated DC-DC converter topology combining a super-lift Luo converter with inductor-capacitor voltage multipliers (VMCs) to achieve high voltage gain without extreme duty cycles. The proposed design offers seven key advantages. These are a continuous input current that reduces input capacitor stress, a common ground between source and load that mitigates EMI, enhanced voltage-lift effect via hybrid Luo-VMC stages, a semiconductor voltage stress that is significantly lower when compared to output voltage, a semiconductor current stress below input current, minimized current stress for most switches and a scalable voltage gain suitable for high-output applications. The converter is analyzed in both ideal and non-ideal modes with derived equations for continuous and discontinuous conduction modes (CCM/DCM). A 100W prototype (12 V input, 312 V output, 50% duty cycle) validated the design showing its efficacy for high-intensity discharge (HID) lamps and other high-gain applications.

Abbreviations

Vin	Input voltage source	$V_{C1} - V_{C7}$	capacitor voltage 1st to 7th
V_{CO}	Output capacitor voltage	$I_{L1} - I_{L3}$	inductor average current 1st to 3rd
$I_2 - I_8$	capacitor inrush current 2nd to 8th	$Vs1$	Voltage stress of the switch
$V_{D1} - V_{D10}$	Voltage stress of the 1st diode to 10th	$I_{D1} - I_{D10}$	Current stress of the 1st diode to 10th
I_{S1}	Current stress of the 1st switch	fs	Switching frequency
P_L	Conduction loss of the inductors	P_{SC}	Conduction loss of the switch
P_D	Conduction loss of the diodes	r_L	The equivalent resistance of the inductors
r_{SC}	The equivalent resistance of the switch	V_{DF}	Threshold voltage of the diodes
η	Efficiency	R	Load
D	Duty cycle	I_O	Output current
δ	The ratio of the activation time of the last diode over the switching period		

I. Introduction

Isolated and non-isolated topologies are the two main groups of DC-DC converters [1]. The isolated DC-DC converters use a high-frequency transformer to provide a high voltage gain [2]. Also, the provided isolation between load and input source protects the sensitive loads from the faults of the input side [3]. All these advantages are accompanied by some disadvantages. Using the transformers increases the volume and mass and decreases the power density of the converter [4]. Additionally, the leakage inductance of the coils leads to the existence of residual currents, which increases the voltage stress of the switch and requires the use of snubber circuits, which increases the complexity of the converter [5]. Consequently, non-isolated topologies can be used in applications that do not require the isolation of the load and input source [6]. Among the classic non-isolated step-up DC-DC converters, the boost and super lift Luo converters are the most popular ones [7]. These converters have a step-up behavior in all duty cycles. However, providing a ten times voltage gain requires using a high value of the duty cycle,

which is close to unity. Such a high value of the duty cycle leads to a poor efficiency, dramatic high semiconductor voltage stress and a reverse recovery time problem of the diodes [8]. Consequently, new and improved topologies are required.

[9]-[22] include recently proposed improved topologies. The presented topology in [9] uses a boost and buck-boost topology to provide a higher voltage gain than the classic converters. Additionally, the continuity of the input current is present. However, the output polarity is reversed. Additionally, the switch number becomes two and a voltage higher than the output voltage is applied to the last switch and diode. Notably, the voltage gain can cause high values as the duty cycle percentage approaches unity. The presented topologies in [10] and [11] use the same idea. Both topologies use a boost and a super lift Luo converter in their structure. Notably, the proposed topology in [10] is a single-switch form of [11]. The voltage gain provided by these topologies is higher than that of the cascaded boost converter while all the semiconductors' voltage stresses are less than the output voltage. Moreover, the continuity of the input current is maintained. Besides all these advantages, the voltage gain increase is not bold, and the difference between the output voltage and the highest voltage stress is not very significant. The proposed topology in [12] combines two boost topologies providing a higher voltage gain than the cascaded boost topology. Although the continuity of the input current is present, it has one more switch and last diode, and the switch in this topology experiences a voltage stress more than the output voltage compared with the cascaded boost topology. The presented topology in [13] is another two-switch topology, which uses a boost and super lift Luo converter. The voltage gain is more than the provided voltage gain by the cascaded connection of the boost and super lift Luo converter. However, this voltage gain is not significantly high and cannot be more than 10 times, while the duty cycle percentage is at low values. [14] presents a topology whose voltage gain is twice that of the cascaded boost topology. All the bold points and the drawbacks of the boost topology are present in this topology. The voltage gain provided in [15] is the same as that provided in [14], with a smaller number of inductors and all the advantages of the boost converter are present in this topology. However, similar to the boost converter, the highest voltage stress of the semiconductors is the same as the output voltage. The presented topologies in [17], [18] employ boost, super lift Luo, and inductor-based circuits to provide a high voltage gain. Both topologies provide a 10 times voltage gain as the duty cycle reaches 50%. All the positive characteristics of the sub topologies are present in the main topologies and all the semiconductors' voltage stress are less than the output voltage. However, the difference is not much significant. These advantages and disadvantages are repeated in [19]. The provided voltage gain by [19] is particularly higher than in [17], [18]. The presented topologies in [20], [21] are improved from of the presented topology in [12]. These converters can provide a voltage gain of more than 10 times while the duty cycle has low values. All the expressed bold points in [12] are present in [20], [21]. Additionally, the challenge of the semiconductors' voltage stress has been solved in [20], [21]. However, employing two switches in the power circuit is still a challenge. The presented topology in [22] is an improved form of the cascaded boost and Cuk converters. The voltage gain is well-increased while utilizing a single-switch structure. However, two problems arise in this topology, the first is the reversed output polarity of the converter and the second is the maximum voltage stress of the semiconductors, which becomes twice the output voltage.

This study presents a new topology of high gain, non-isolated DC-DC converters. The merits of this topology are: (I) the continuity of the input current is provided to reduce the current stress of the input filter capacitor; (II) the common ground of the load and the input source is present to reduce the electromagnetic interference (EMI) problems; (III) super lift Luo converter is used beside the inductor-based and capacitor-based voltage multiplier cells (VMC) to improve the voltage-lift technique; (IV) the voltage stress of the semiconductors is less than the output voltage with a bold difference; (V) the current stress of the semiconductors is less than the input current; (VI) most of the semiconductors experience the lowest current of the converter as their current stress; (VII) the voltage gain of the converter has increased appropriately that can easily provide the higher voltage gains without the high percentage of the duty cycle. The former characteristics makes this topology demanding for high-intensity discharge (HID) lamps and water electrolysis.

In the rest of this article, the proposed topology will be given in Section II. Section III represents operating modes' analysis. Section IV discuses non-ideal voltage gain and section V considers efficiency. Section VI includes comparative analysis and Section VII demonstrated the proposed topology application. Section VIII deals with small signal analysis and section IX experimental results. Finally, the conclusion is drawn in Section X.

II. Proposed Topology

A. Circuit Description & Operation Overview

In this section, the operation of the converter and its theoretical relations to the various parameters are discussed in the ideal and continuous conduction modes. As illustrated in Fig. 1, the positive output super lift Luo converter (POSLLC) represents an enhanced version of boost topology. This figure depicts the voltage lift process occurring between the input source and the initial capacitor. Essentially, the input source and the first capacitor are connected in parallel during the first operating phase. In the second phase, they are connected in series with the inductor, which increases the voltage gain. Although the voltage gain from this topology surpasses that of

a traditional boost converter, the enhancement is modest. Therefore, it is essential to amplify the impact of the voltage lift method. One effective approach to achieving this is through VMC. Figure 2 illustrates the integration of a VMC with POSLLC, where the VMC replaces the inductor in the POSLLC setup. Utilizing a VMC enhances the voltage gain of the sub-converter. Furthermore, employing inductor-based VMCs reduces the conduction losses by splitting a defined current across two inductors rather than a single one. Additionally, another VMC can be incorporated to achieve a higher voltage gain. As shown in Fig. 3, a diode-capacitor VMC can complement the configuration presented in Fig. 2. This type of VMC not only boosts voltage gain but also increases the separation between the switch and the output terminal, thereby reducing voltage stress on the semiconductors. The configuration in Fig. 3 offers the final iteration of the enhanced POSLLC, featuring two additional voltage-lift processes compared to the conventional POSLLC. However, this new configuration also raises the input current ripple. To address this issue, a boost topology is integrated into the design shown in Fig. 3. Figure 4 illustrates the proposed topology of this study. The inclusion of the boost converter at the start of the proposed configuration ensures continuous input current with minimal ripple. Additionally, the overall voltage gain of the topology takes a quadratic form, further supporting the voltage lift method. It is important to highlight that the entire design is centered around a switch with a straightforward drive structure. In the steady state, the system operates in two modes. During the first mode, as depicted in Fig. 5(a), the switch, diodes two through five, the seventh diode, and the ninth diode are engaged, resulting in a positive voltage being applied to the inductors. Consequently, the inductors become magnetized and store energy within their field.

In the second operating mode, the semiconductors that were active in the first mode turn off, while the remaining semiconductors are activated. Figure 5(b) illustrates the equivalent circuit for this mode. A negative voltage is applied to the inductors to cause demagnetization. It's important to highlight that in the first operating mode, the first through third capacitors are in parallel, along with the series connection of the third and fifth capacitors to the fourth capacitor and the series connection of the fourth, sixth and seventh capacitors to the output capacitor. In the second mode, the sixth capacitor becomes parallel with the seventh and the fourth through sixth capacitors are in series with the output capacitor. Based on the discussed concepts and the shown equivalent circuits, the equations for the inductors' voltage and the capacitors' current are as follows:

$$\begin{cases} V_{L1} = D\left(V_{in}\right) + \left(1-D\right)\left(V_{in} - V_{C1}\right) \\ V_{L2} = D\left(V_{C1}\right) + \left(1-D\right)\left(V_{C1} + V_{C2} - V'\right) \\ V_{L3} = D\left(V_{C1}\right) + \left(1-D\right)\left(V' + V_{C3} - V_{C4}\right) \end{cases} \quad (1)$$

$$V_{C1} = V_{C2} = V_{C3} \quad (2)$$

$$V_{C3} + V_{C5} = V_{C4} \quad (3)$$

$$V_{C6} = V_{C7} \quad (4)$$

$$V_o = V_{C4} + V_{C6} + V_{C7} \quad (5)$$

$$V_o = V_{C4} + V_{C5} + V_{C7} \quad (6)$$

$$\begin{cases} i_{C1} = D\left(-i_{L2} - i_{L3} - i_2 - i_3\right) + \left(1-D\right)\left(i_{L1} - i_{L2}\right) \\ i_{C2} = D\left(i_2\right) + \left(1-D\right)\left(-i_{L2}\right) \\ i_{C3} = D\left(i_3 + i_4 + i_8\right) + \left(1-D\right)\left(-i_{L2}\right) \\ i_{C4} = D\left(-i_4\right) + \left(1-D\right)\left(i_{L2} - i_5\right) \\ i_{C5} = D\left(i_4 + i_8\right) + \left(1-D\right)\left(-i_5\right) \\ i_{C6} = D\left(i_8\right) + \left(1-D\right)\left(i_7 - i_5\right) \\ i_{C7} = D\left(i_8\right) + \left(1-D\right)\left(-i_7\right) \\ i_{Co} = D\left(-i_8 - I_o\right) + \left(1-D\right)\left(i_5 - I_o\right) \end{cases} \quad (7)$$

Notably, the second and third inductors become series with each other in the second operating point. Consequently, their average current gets a relation as follows:

$$i_{L2} = i_{L3} \quad (8)$$

It is important to note that i2, i3, i4, i5, i7, and i8 are the capacitors' created inrush currents during their parallel connection.

Utilizing the voltage second balance in the inductors' voltage equation yields the average voltage of the capacitors as follows:

$$\begin{cases} V_{C1} = V_{C2} = V_{C3} = \dfrac{V_{in}}{1-D}, V' = \dfrac{2-D}{\left(1-D\right)^2} V_{in} \\ V_{C4} = \dfrac{3-D}{\left(1-D\right)^2} V_{in}, V_{C5} = V_{C6} = V_{C7} = \dfrac{2}{\left(1-D\right)^2} V_{in} \end{cases} \quad (9)$$

According to the expressed relations in (5), (6), and (9) the resulting voltage gain is as follows:

$$V_o = \frac{7-D}{\left(1-D\right)^2} V_{in} \quad (10)$$

the extracted voltage gain results from both the quadratic and voltage-lift methods. Furthermore, the voltage-lift The extracted voltage gain results from both the quadratic and voltage-lift methods. Furthermore, the voltage-lift technique is shown to have a threefold impact compared to the traditional POSLLC. Figure 6 illustrates a comparison between the voltage gain of the proposed topology and that of the classic boost converter. It is evident that the proposed topology achieves a higher voltage gain at lower duty cycle percentages than the boost topology does at higher duty cycle percentages. In other words, it is not required to use the higher percentages of the duty cycle to provide a significant value of the voltage gain. Notably, this point becomes bold, when the reverse recovery time of the semiconductors is an issue. This

achievement is the first one compared with the classic boost converter.

Using the current second balance in the capacitors' current equation results in the average current for the inductors and inrush currents as detailed below:

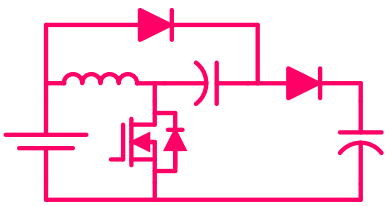

Fig. 1. Classic POSLLC.

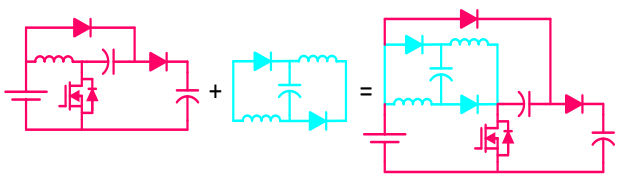

Fig. 2. Improving a classic POSLLC with an inductor-based VMC.

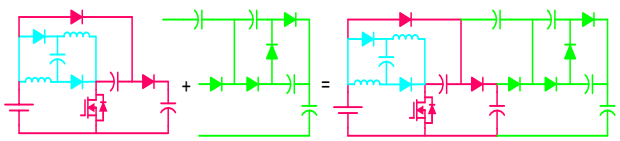

Fig. 3. Improving the modified POSLLC with a diode-capacitor VMC.

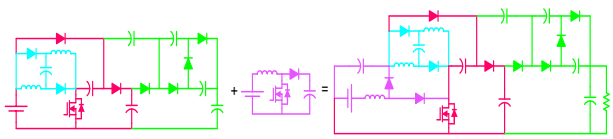

Fig. 4. Building procedure of the proposed topology.

$$\begin{cases} i_{L1}=\dfrac{7-D}{(1-D)^2}I_o, i_{L2}=i_{L3}=\dfrac{3}{1-D}I_o, i_2=\dfrac{3}{D}I_o \\ i_3=i_4=i_8=\dfrac{I_o}{D}, i_5=\dfrac{2}{1-D}I_o, i_7=\dfrac{I_o}{1-D} \end{cases} \quad (11)$$

Calculating the average current of inrush currents in inductors and capacitors helps define the current stresses in semiconductors.

$$\begin{cases} I_S=\dfrac{6+D-D^2}{(1-D)^2}I_o, I_{D1}=\dfrac{7-D}{1-D}I_o, I_{D2}=\dfrac{7D-D^2}{(1-D)^2}I_o \\ I_{D3}=I_{D4}=\dfrac{3}{1-D}I_o, I_{D5}=\ldots=I_{D10}=I_o \end{cases} \quad (12)$$

According to the expressed equations, 60% of the semiconductors experience the lowest current value as their current stress. Moreover, 80% of the semiconductors have a negligible current stress, which keeps the semiconductors' conduction loss at a desired low value. Notably, employing the diode-capacitor circuit at the end of the proposed topology leads to the equality of the current stress of 6 diodes to the output power. Such a feature is independent of the diodes' type. Calculating the average voltage across the capacitors is essential for assessing the voltage stress on the semiconductors, as outlined below:

$$\begin{cases} V_{D5}=V_{D6}=V_{D7}=V_{D8}=V_{D9}=V_{D10}=\dfrac{2}{(1-D)^2}V_{in}, V_S=\dfrac{2}{(1-D)^2}V_{in} \\ V_{D3}=V_{D4}=\dfrac{V_{in}}{(1-D)^2}, V_{D2}=\dfrac{1+D}{(1-D)^2}V_{in}, V_{D1}=\dfrac{V_{in}}{1-D} \end{cases} \quad (13)$$

The analyzed values indicate that semiconductors do not face a voltage exceeding the output voltage. Notably, the use of the diode-capacitor circuit at the end of the converter leads to a voltage stress, which is one-third of the output voltage on the switch and the last 5 diodes. Such a feature is independent of the diode types and based of the structure of the diode-capacitor circuit. Additionally, their current does not surpass the input current. Based on this, Figure 7 presents the semiconductors' normalized voltage/current stress. The figure indicates that the maximum normalized voltage stress for the semiconductors is 0.33. Furthermore, the maximum current stress is associated with the switch, which has a normalized voltage stress below one. Moreover, most diodes show a voltage stress of less than 0.1. These values illustrate that the semiconductors operate within acceptable limits in the proposed topology. Figure 8 presents the same analysis for the boost converter. According to this figure, the maximum of the normalized voltage stress of the semiconductors is the same as the unity. This result is not desired and has been solved in the proposed topology. Notably, 70 % of the semiconductors in the proposed topology has a normalized current stress less than 40% in all duty cycle percentages. However, such a bold point is absent in the classic boost converter.

The simplified form of the inductors' current ripple according to the inductors' voltage equation and capacitors'

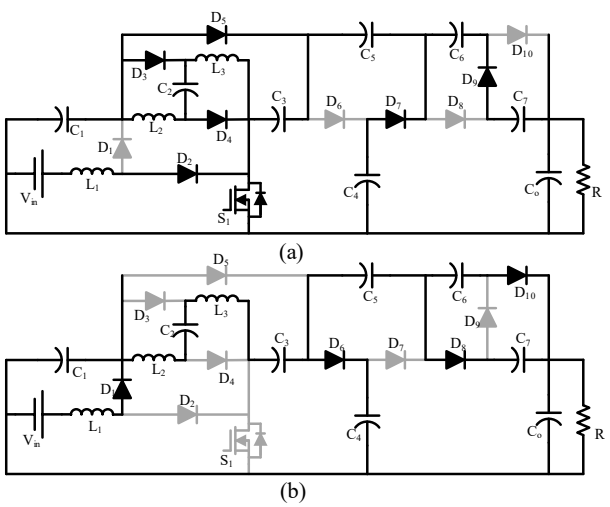

Fig. 5. Equivalent circuit of the proposed topology: (a) first mode, (b) second mode.

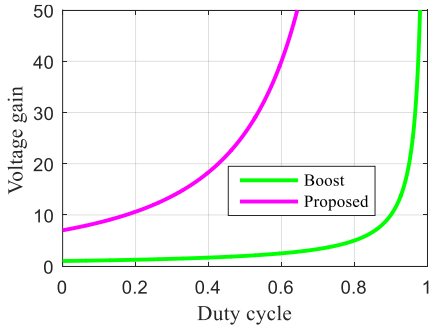

Fig. 6. Voltage gain comparison of the proposed topology and classic boost converter.

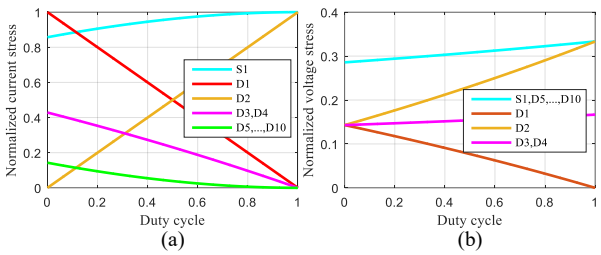

Fig. 7. Proposed converter's semiconductors normalized: (a) current stress, (b) voltage stress

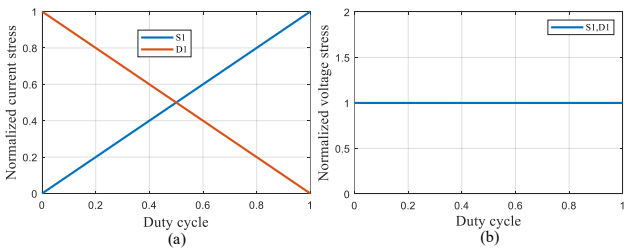

Fig. 8. Boost converter's semiconductors normalized: (a) current stress, (b) voltage stress

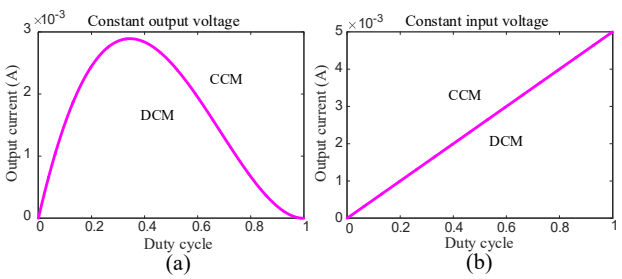

Fig. 9. The operational region of the converter between CCM and DCM is determined according to the output current and duty cycle, while (a) the output voltage is constant and (b) the input voltage is constant.

voltage ripple according to the capacitors' current equation are as follows:

$$\begin{cases} \Delta i_{L1}=\dfrac{DV_{in}}{L_1 f_s},\Delta i_{L2}=\dfrac{DV_{in}}{(1-D)L_2 f_s},\Delta i_{L3}=\dfrac{DV_{in}}{(1-D)L_3 f_s},\Delta v_{C1}=\dfrac{(4+2D)I_o}{(1-D)C_1 f_s},\Delta v_{C2}=\dfrac{3I_o}{C_2 f_s} \\ \Delta v_{C3}=\dfrac{3I_o}{C_3 f_s},\Delta v_{C4}=\dfrac{I_o}{C_4 f_s},\Delta v_{C5}=\dfrac{2I_o}{C_5 f_s},\Delta v_{C6}=\dfrac{I_o}{C_6 f_s},\Delta v_{C7}=\dfrac{I_o}{C_7 f_s},\Delta v_{Co}=\dfrac{(1+D)I_o}{C_o f_s} \end{cases} \quad (14)$$

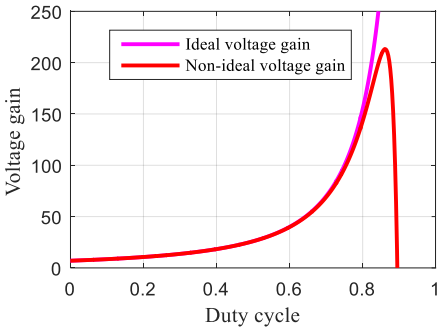

Fig. 10. Voltage gain comparison of the proposed topology in the ideal and non-ideal mode.

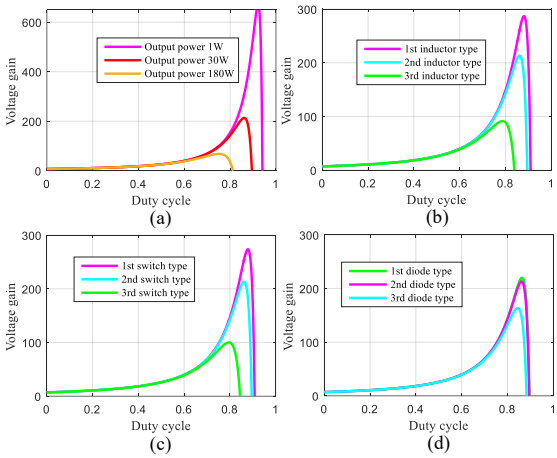

Fig. 11. Voltage gain of the proposed converter in the non-ideal mode according to the change of: (a) output power, (b) inductors' core type, (c) switch type, and (d) diodes' type.

III. Operating-Mode Analysis

The operation of the converter in the continuous and discontinuous conduction modes is not the same. Consequently, the effective factors in changing the continuous conduction mode to the discontinuous conduction mode are discussed. To maintain continuous conduction mode (CCM), the current ripple in the inductors must remain under twice the average current of each inductor. The value of the inductors directly influences their current ripple. Based on this criterion, the minimum inductor value necessary for sustaining CCM is as follows:

$$L_1 > \frac{D(1-D)^4 R}{2(7-D)^2 f_s}, L_2 > \frac{D(1-D)^2 R}{6(7-D) f_s}, L_3 > \frac{D(1-D)^2 R}{6(7-D) f_s} \quad (15)$$

Although the value of the inductors remains constant, their average current plays a crucial role in the converters' performance in CCM. To maintain CCM, the average current through the inductors needs to exceed half of their current ripple. This average current is determined by both the duty cycle and the average output current. Therefore, the converter's operational region between CCM and Discontinuous Conduction Mode (DCM), given constant input and output

voltages, can be represented as shown in Fig. 8, based on the equations provided below:

$$I_o = \frac{D(1-D)^2}{7-D}\frac{V_o}{6L_3 f_s} = D\frac{V_{in}}{6L_3 f_s} \tag{16}$$

All points above the presented curves are part of the CCM, while those below the curves refer to the DCM. The points on the curves represent the boundary condition.

The extracted voltage gain and average voltage of the capacitors in the DCM is as follows:

$$\begin{cases} V_{C1} = V_{C2} = V_{C3} = \dfrac{D+\delta}{\delta}V_{in} \\ V_{C4} = \dfrac{(D+\delta)(2D+3\delta)}{\delta^2}V_{in} \\ V_{C5} = V_{C6} = V_{C7} = 2\left(\dfrac{D+\delta}{\delta}\right)^2 V_{in} \\ \dfrac{V_o}{V_{in}} = \dfrac{(D+\delta)(6D+7\delta)}{\delta^2} \end{cases} \tag{17}$$

In this equation, D refers to the ratio of the activation time of the switch over the whole period of switching and δ refers to the ratio of the activation time of the last diode over the whole switching time period.

IV. Small Signal Analysis

In this section, the state space equations are discussed to extract a suitable compensator for the proposed topology in the closed-loop system. In order to analyze the stability of the proposed converter, the space state matrices have been presented in this section. It is good to note that the independent inductors are two as well as the independent capacitors. According to this concept, the space state matrices are as follows:

$$\frac{d}{dt}\begin{pmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{Co} \end{pmatrix} = \begin{pmatrix} 0 & 0 & \dfrac{D-1}{L_1} & 0 \\ 0 & 0 & \dfrac{3-D}{2L_2} & \dfrac{D-1}{3L_2} \\ \dfrac{1-D}{3C_1} & \dfrac{D-3}{3C_1} & 0 & \dfrac{-2}{3RC_1} \\ 0 & \dfrac{1-D}{2C_o} & 0 & \dfrac{-1}{2RC_o} \end{pmatrix}\begin{pmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{Co} \end{pmatrix} + \begin{pmatrix} \dfrac{V_{C1}}{L_1} \\ \dfrac{\frac{1}{3}V_{CO} - \frac{1}{2}V_{C1}}{L_2} \\ \dfrac{-I_{L1}+I_{L2}+4I_o}{C_1} \\ \dfrac{-I_{L2}}{C_o} \end{pmatrix} d$$

$$y = \begin{pmatrix} 0 & 0 & 0 & 1 \end{pmatrix}\begin{pmatrix} i_{L1} \\ i_{L2} \\ v_{C1} \\ v_{Co} \end{pmatrix}$$

According to these equations and using MATLAB, the bode diagram of the proposed topology have been extracted and presented in Fig. 12(a). It can be understood that the phase and gain margins are negative which stands from the non-minimum phase behavior of the proposed topology. Also, their multiplication is positive which shows the stability. In order to solve the non-minimum phase behavior, a suitable compensator must be designed. Using SISOTOOL of MATLAB leads to a compensator as follows:

$$G_C(s) = \frac{0.194}{s}$$

Applying this compensator to the plant leads to the positive phase/gain margins of the proposed topology according to Fig. 12(b).

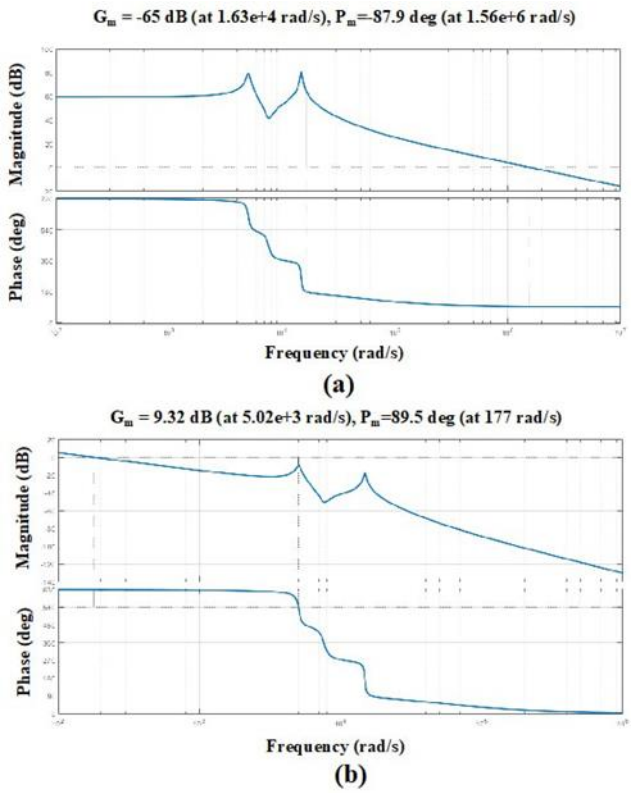

Fig. 12. Bode Diagram of the proposed topology: (a) before compensating (b) after compensating.

V. Performance Evaluation

A. Non-Ideal Voltage Gain

This sub-section considers the non-ideal analysis of the converter. The voltage gain extracted in the previous section corresponds to an ideal scenario where components are free from parasitic elements. However, this relationship cannot accurately forecast voltage gain behavior under varying conditions and differing component qualities. The parasitic elements of the inductors, switch, and diodes (r_L, r_S, and r_D) were considered to derive a more precise expression for non-ideal voltage gain. The simplified voltage gain relationship for the converter in non-ideal mode is as follows:

$$\frac{V_o}{V_{in}} = \frac{7-D}{(1-D)^2}\left(1 - \frac{r_L}{R}\frac{7-D}{(1-D)^4} - \frac{r_S}{R}\frac{D(7-D)}{(1-D)^4} - \frac{r_D}{R}\frac{7-D}{(1-D)^3}\right) \tag{18}$$

The extracted relation reveals additional components that are missing in the ideal mode's corresponding relation. These components contribute to the variations in voltage gains between the ideal and non-ideal modes. Figure 10 illustrates

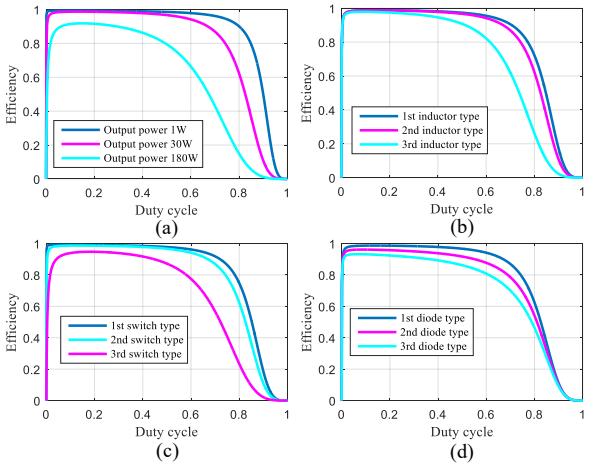

Fig. 13. Efficiency of the proposed converter in the non-ideal mode according to the change of: (a) output power, (b) inductors' core type, (c) switch type, and (d) diodes' type.

the voltage gain of the proposed topology in both the ideal and non-ideal component modes. Notably, the voltage gain of the converter peaks in the non-ideal mode, a feature absenting in its ideal model counterpart. The equation derived for the ideal mode indicates that higher duty cycle percentages correlate with increased voltage gain values. Conversely, the equation for the non-ideal mode does not support this expectation. Another significant observation from the figure is that both curves align at low duty cycle percentages, suggesting that higher voltage gains occur at lower duty cycles in both ideal and non-ideal conditions. Thus, the converter should be designed to deliver higher voltage gains at low-duty cycle percentages. Importantly, voltage gain characteristics vary under different conditions. Figure 11 demonstrates how voltage gain behaves based on output power and component quality variations. Figure 11(a) shows that lower output powers allow for a broader range of alignment between ideal and non-ideal voltage gains. Figures 11(b)-(d) illustrate that the sensitivity of voltage gain in the non-ideal mode remains consistent regardless of changes in inductor and switch types. Additionally, the sensitivity of voltage gain regarding diode-type changes is lower than the others.

B. *Efficiency*

Based on the analyzed relationships between the average current of inductors and the average voltage of capacitors, the input and output powers are equal, assuming ideal conditions for circuit components. However, in practical scenarios, the components are imperfect, resulting in lower output power than input power due to associated losses. This study accounts for the conduction losses of inductors (P_L), switches (P_{SC}), and diodes (P_D), while disregarding frequency losses related to low switching frequencies. The following is a summary of these simplified losses:

$$\begin{cases} P_L=\sum_{k=1}^{3} r_{L_k} i^2_{L_k}=\dfrac{67-50D+19D^2}{(1-D)^4}\dfrac{r_L}{R}P_o, P_{SC}=r_S i^2_S=\dfrac{\left(6+D-D^2\right)^2}{D(1-D)^4}\dfrac{r_S}{R}P_o \\ P_D=\sum_{k=1}^{3} V_{DF_k} i_{D_k}=\dfrac{18-18D+6D^2}{(1-D)^2}V_{DF}I_o, \eta=\dfrac{P_o}{P_o+P_L+P_{SC}+P_D} \\ Max\left\{r_{L_k}\right\}=r_L, Max\left\{V_{DF_k}\right\}=V_{DF} \end{cases} \quad (19)$$

The equations indicate that efficiency behavior is influenced by output power, component quality and duty cycle percentage. Figure 13 illustrates efficiency changes based on variations in the output power and the types of components. The most significant impact arises from changes in the output power. In the second stage, the type of switch holds the most essential effect. Following this, the third stage involves changes in diode types, while the least influence comes from changes in the inductor core type. Significantly, altering the diode type strongly affects the various component changes, even at low duty cycle percentages.

C. *Comparative Analysis*

In this sub-section, the bold features and achievements of the proposed topology are compared with the recently suggested converters. One of the outstanding features of the proposed topology is the high gain of voltage. As outlined in previous sections, this gain is achieved by integrating quadratic converters and voltage lift circuits. As a result, there's no need to utilize high-duty cycle to attain a substantial voltage gain. Figure 14 compares voltage gains among the proposed topology and the converters introduced in references [5]-[47] which indicates that the voltage gain from the proposed topology exceeds that of [5]-[47] across all duty cycle percentages including lower and higher duty cycles. This comparison highlights the considerable superiority of the proposed topology over currently suggested converters. Increasing the component number is achieved by providing a high value of the voltage gain. Therefore, the concept of the voltage gain density must be defined to see the voltage gain and the components number increase simultaneously. Figure 15(a) illustrates the voltage gain density over the whole number of components. According to this figure, the proposed topology in this study has the highest voltage gain density in all duty cycle percentages. Notably, such superiority is repeated in the voltage gain density over the inductor number (Fig. 15(b)), capacitor number (Fig15(c)), and switch number (Fig. 15(d)). In the case of voltage gain density over the diodes' number, the proposed topology is the second top converter among the recently proposed converters. Table 1 compares the number of components, voltage gain and the maximum value of the switch and diode voltage stress of the proposed topology with presented converters in [9]– [22]. According to this table, the proposed topology has the highest value of voltage gain. Additionally, the maximum voltage stress of the switch and diodes are much less than the output voltage. Notably, the

expressed data in column 1 to column 6 of this table, have been used in Fig. 15. To have a better view from the advantage of the proposed topology, the expressed voltage stresses in the seventh and eighth columns have been normalized by the expressed output voltages in the sixth column and relevant results have been presented in Fig. 16. According to Fig. 16 the proposed topology has the lowest normalized voltage stress. In other words, beside the high voltage gain of the proposed topology, the highest voltage stress of the semiconductors in this converter, is less than the output voltage with the highest difference. Such an advantage makes this converter suitable for high DC voltage applications.

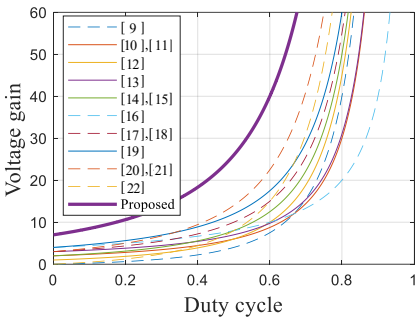

Fig. 14. Voltage gain comparing of the proposed topology with the presented topologies in [9]-[22].

TABLE 1 THE COMPARISON OF PROPOSED CONVERTER WITH THE STATE-OF-THE-ART CONVERTERS

	L	C	S	D	ALL	Voltage gain	Max (V_S)	Max (V_D)
[9]	2	3	2	3	10	$\frac{2D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$
[10]	2	3	1	4	10	$\frac{2-D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$
[11]	2	3	2	3	10	$\frac{2-D}{(1-D)^2}V_{in}$	$\frac{2-D}{(1-D)^2}V_{in}$	$\frac{2-D}{(1-D)^2}V_{in}$
[12]	2	3	2	3	10	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[13]	2	3	2	3	10	$\frac{3-3D+D^2}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{2-D}{(1-D)^2}V_{in}$
[14]	3	5	1	5	14	$\frac{2}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$
[15]	2	4	1	5	12	$\frac{2}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$
[16]	2	4	2	4	12	$\frac{4}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[17]	3	6	1	6	16	$\frac{3-D}{(1-D)^2}V_{in}$	$\frac{V_{in}}{(1-D)^2}$	$\frac{V_{in}}{(1-D)^2}$
[18]	3	4	1	6	14	$\frac{3-D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[19]	3	4	1	6	14	$\frac{2(2-D)}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[20]	2	5	2	5	14	$\frac{3+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[21]	2	5	2	5	14	$\frac{3+D}{(1-D)^2}V_{in}$	$\frac{1+D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$
[22]	4	6	2	7	19	$\frac{4D}{(1-D)^2}V_{in}$	$\frac{4}{(1-D)^2}V_{in}$	$\frac{4}{(1-D)^2}V_{in}$
Proposed	3	8	1	10	22	$\frac{7-D}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$	$\frac{2}{(1-D)^2}V_{in}$

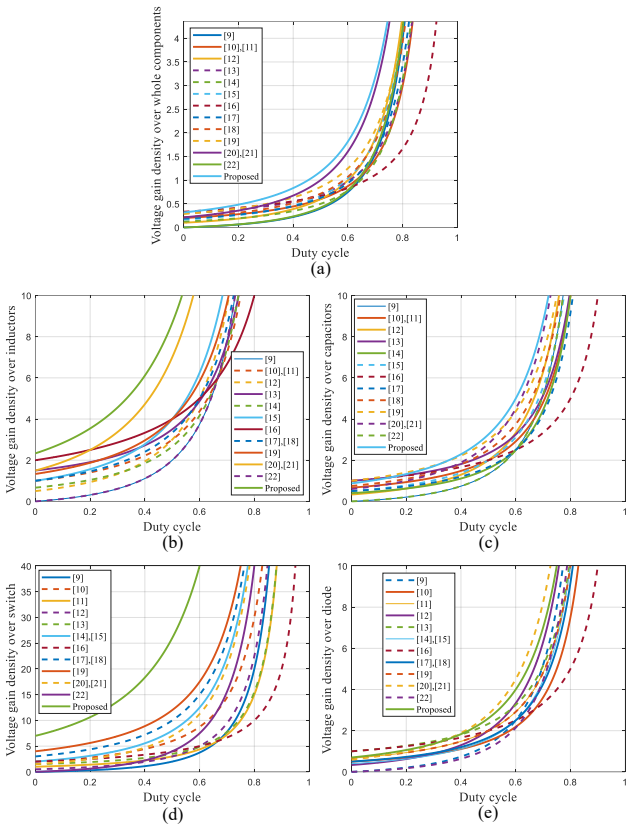

Fig. 15. Voltage gain density over:
(a) whole components, (b) inductors' number, (c) capacitors' number, (d) switches' number and (e) diodes' number.

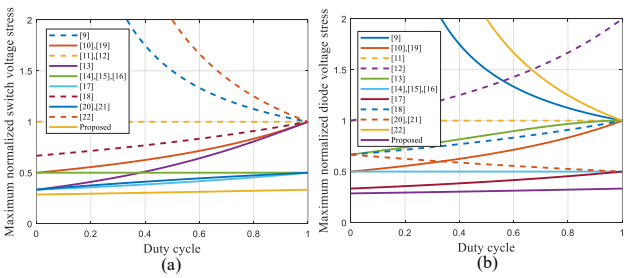

Fig. 16. Comparing the maximum normalized voltage stress of: (a) switches, (b) diodes.

VI. Application Case Studies

This section explains the suitable applications in which the proposed topology can be employed.

A. HID Lamps

According to the extracted voltage gain in the second section, providing a high voltage gain by the low duty cycle percentage is one of the bold achievements of the proposed topology. Such a high voltage gain can be used in applications such as HID lamps and Hydrogen extraction. HID lamps require a high voltage at their input side with a negligible input current. However, the accessible batteries in cars can provide a low voltage (12V) and high current. Consequently, a high-gain DC-DC converter (same as the proposed topology) can be

used according to Fig. 17 to provide the required input voltage of the HID lamps.

B. Hydrogen Extraction

It is good to note that the proposed topology can be used to electrolyze the water to extract the hydrogen as a clean fuel. Such a high voltage gain DC-DC converter can increase the output voltage of the battery or photovoltaic panels to make it suitable for the input side of the pulsed power converter. At the next step, the provided pulsed waveform can be applied to the electrodes, which are surrounded by water and hydrogen and next oxygen can be produced and collected by membranes. Figure 18 presents the symbolic presentation of the mentioned procedure in water refinery applications.

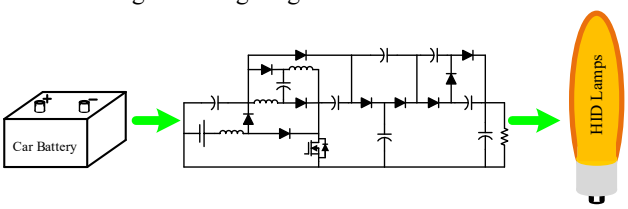

Fig. 17. Application of the proposed topology in HID lamps.

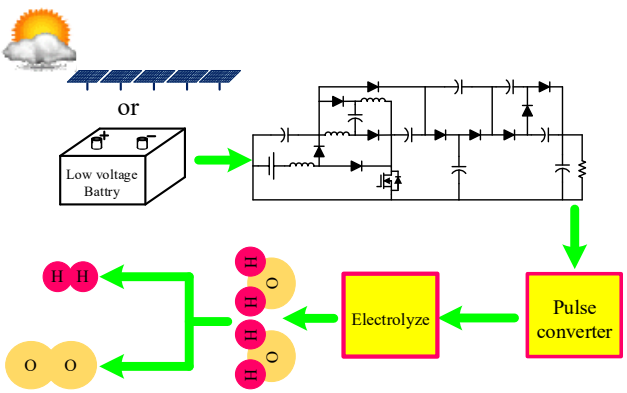

Fig. 18. Application of the proposed topology in hydrogen extraction from water electrolyzer.

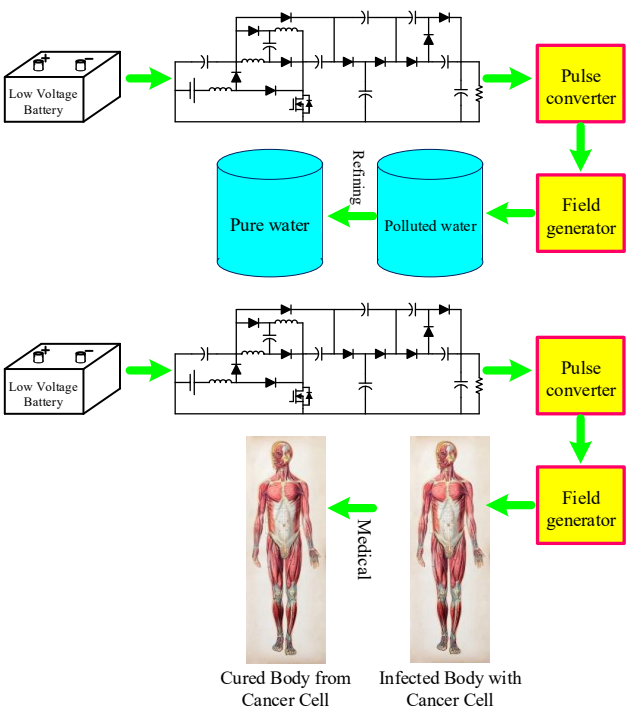

Fig. 19. Application of the proposed topology in medical procedures.

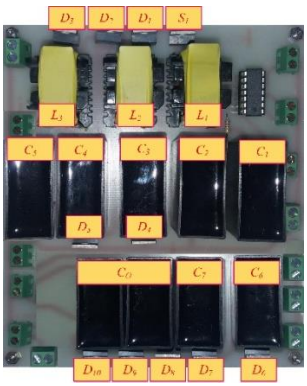

Fig. 20. The prototype of the proposed converter.

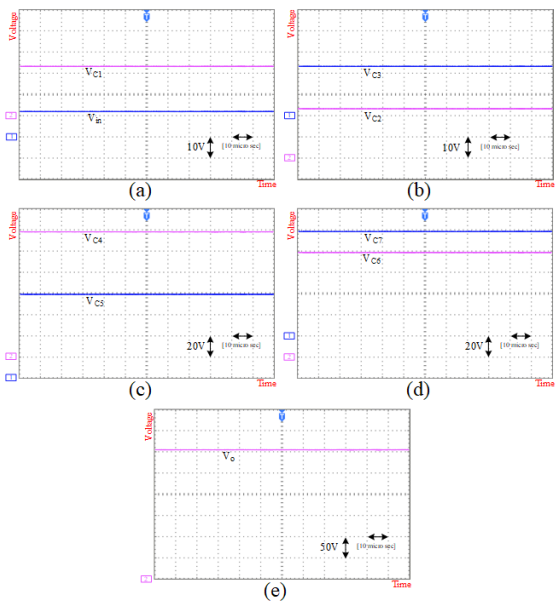

Fig. 21. Experimental outcomes.

C. Medical Procedures

With the aforementioned capability of this converter, beside the pulsed power converter, it can be used in medical procedures technologies. Same as the mentioned application, the same procedure can be employed in the medical applications in the same procedure as Fig. 19.

VII. Experimental Results (Prototype Measurement vs. Simulation)

This section discusses the validity of the extracted relations based on the experimental results. The results are obtained

using the prototype. To create the prototype, it is essential to identify the circuit components. The identification of these components involves defining their current and voltage characteristics. To establish the voltage and current characteristics of the components, one must specify the input voltage, output current and duty cycle. In this study, the parameters are defined in Table 2.

The input voltage value is the same as the car batteries' voltage. The converter's output current is determined according to the input current of the HID lamps. Considering these values and the current/voltage stress of the semiconductors is obtained as Table 3.

TABLE 2 DEFINED PARAMETERS

ITEM	PARAMETER	VALUE
1	V_{in}	12V
2	I_o	0.01A
3	D	0.5

TABLE 3 THE AVERAGE VALUES FOR INDUCTORS, CAPACITORS AND SEMI-CONDUCTORS

ITEM	VALUE	ITEM	VALUE	ITEM	VALUE
I_{L1}	260mA	V_o	312V	V_{D1}	24V
I_{L2}	60mA	V_{C1}	24V	V_{D2}	72V
I_{L3}	60mA	V_{C2}	24V	V_{D3}	48V
I_{S1}	250mA	V_{C3}	24V	V_{D4}	48V
I_{D1}	130mA	V_{C4}	120V	V_{D5} ... V_{D10}	96V
I_{D2}	130mA	V_{C5}	96V	V_S	96V
I_{D3}	60mA	V_{C6}	96V		
I_{D4}	60mA	V_{C7}	96V		
I_{D5}...I_{D10}	10 mA				

TABLE 4 MINIMUM VALUES FOR CAPACITORS AND INDUCTORS

ITEM	VALUE	ITEM	VALUE
L_1	1.5mH	C_3	500nF
L_2	13.3mH	C_4	33.3nF
L_3	13.3mH	C_5	83.3nF
C_o	19.2nF	C_6	41.6nF
C_1	1600nF	C_7	41.6nF
C_2	500nF		

Based on the voltage-current stress of the semiconductors, IRF640 may replace the switch, while FES8GT can be utilized for the diodes. Taking into account 30 percent current ripple for the inductors and 5 percent voltage ripple for the capacitors, the minimum values for the inductors and capacitors are determined as Table 4.

EC-type inductor cores are ideal for this project as they readily provide the required inductances. Additionally, MKT capacitors are perfect for high-frequency applications due to their negligible Equivalent Series Resistance (ESR) and excellent performance.

According to the expressed concepts, the prototype of the proposed topology has been displayed in Fig. 20. The extracted experimental results have been presented in Figs. 21-23. The presented waveforms in Fig. 21 are capacitors and input source voltage waveforms. The current waveform of the inductors, semiconductors and the load have been presented in Fig. 22. The voltage waveforms of the semiconductors have been presented in Fig. 23. Comparing the corresponding waveforms with the expressed values in Table 3, shows their compatibility and also validates the design criteria. Moreover, comparing the highest voltage stress of the semiconductors with the output voltage, demonstrates that the semiconductors' highest voltage stress is one-third of the output voltage. although in the boost converter, using the expressed relations in the second section, the average voltage of the capacitors, the average current of the inductors the highest voltage stress is the same as the output voltage.

Fig. 24 presents the prototype of the boost converter and Fig. 25 demonstrates the voltage waveforms of the capacitor and semiconductors in the boost converter.

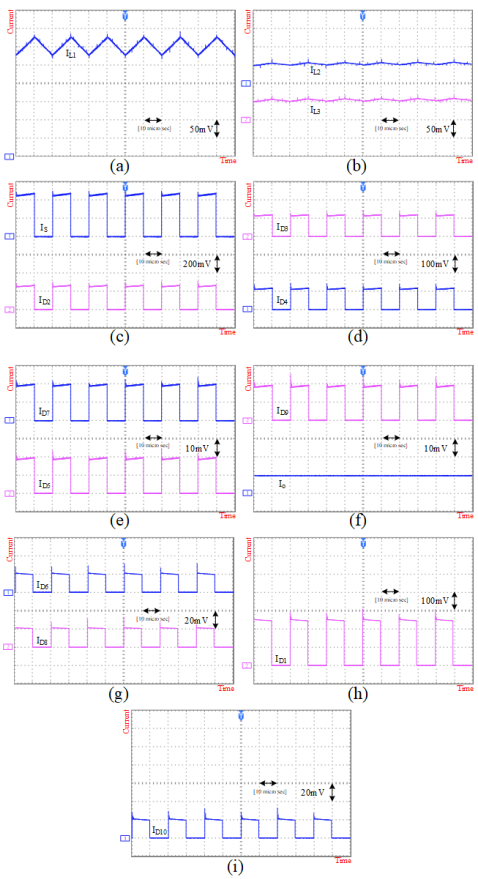

Fig. 22. Experimental outcomes.

Fig. 26 presents the extracted voltage gain of the converter according to the experimental results and the theoretical relation of the voltage gain. According to this figure, while the duty cycle is less than 70%, both curves are compatible with each other and their differences are negligible. While the duty cycle becomes more than 70%, the difference of the curves increases. The reason behind this is due to the employed approximations during the non-ideal voltage gain relation calculations. Notably, this region is not suggested due to the

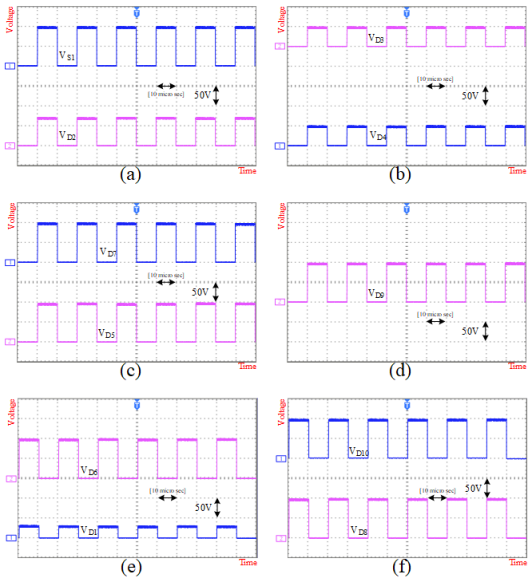

Fig. 23. Experimental outcomes.

low value of efficiency in this region. Fig. 27 presents the efficiency of the converter in a constant duty cycle (50%) and the input/output voltages. In this procedure the load value is changing and causes the power to change. According to this figure, the extracted efficiency is more than 90% at the reported output powers. It is notable that the extracted curve corresponds to high output voltage and low output current conditions. The reason upon the selection of such a condition lies in the application of this converter, which requires high voltage and low current. Moreover, the extracted results can be improved by utilization of high-quality and expensive components.

Fig. 28 presents the behavior of the output voltage according to the change in the load during a constant input voltage. According to this figure, during the load changing, the output voltage keeps its value and does not see any change. Such a result shows the accuracy of the designed controller in the small signal analysis. Consequently, the output voltage is robust according to the change in the load.

VIII. Conclusion

In this study, a non-isolated DC-DC converter was introduced. This topology provided a 26 times voltage gain with a 50 percent duty cycle by employing only one switch. This achievement showed the capability of the proposed topology in providing high voltage gain. Additionally, the benefits of traditional step-up converters were maintained while addressing their shortcomings. The high voltage gain and minimizing the voltage stress on the semiconductors, with the maximum voltage stress being one-third of the output voltage, were achieved. The experimental results were gathered and compared against design parameters, confirming the compatibility of all theoretical models and principles. The extracted compatibility between results and theoretical relations showed that the proposed topology can be employed with the mentioned application and achieves acceptable outcomes.

In order to reduce the EMI and electromagnetic compatibility (EMC), zero voltage switching (ZVS) and zero current switching (ZCS) techniques can be done. In the future study, the restructuring of the proposed topology with ZVC and ZCS will be considered. Moreover, the prototyping considerations such as Minimizing High di/dt Loops, Ground Plane Designing, putting noisy components (MOSFETs, diodes) away from sensitive analog circuits and placing ceramic capacitors close to switching devices to suppress high-frequency noise can be done. Furthermore, filtering techniques and shielding and grounding methods must be done with a detailed attention.

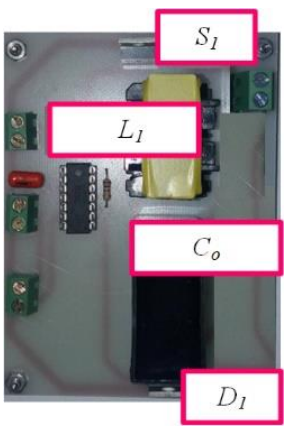

Fig. 24. Conventional boost converter.

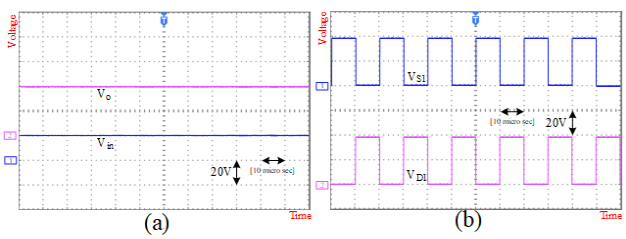

Fig. 25. Experimental results of the boost converter: (a) output voltage and input voltage, (b) Voltage waveforms of the semiconductors.

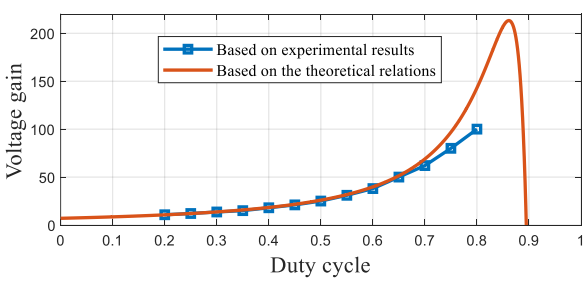

Fig. 26. Voltage gain of the converter according to the experimental results.

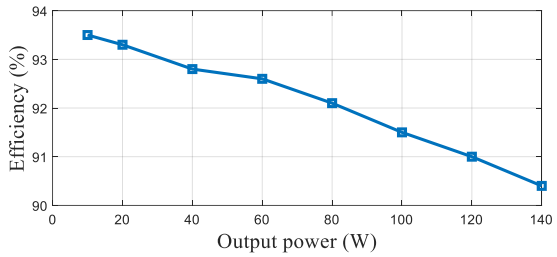

Fig. 27. Efficiency of the converter according to the experimental results.

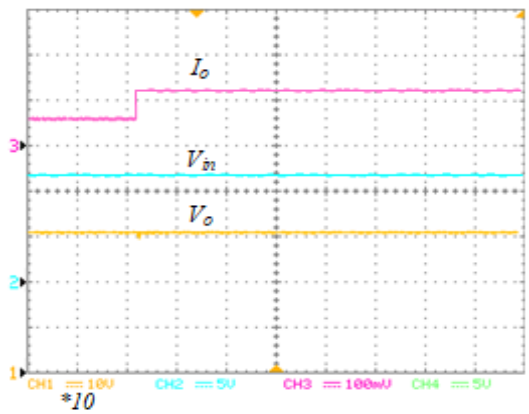

Fig. 28. Dynamic behavior of the proposed topology.

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