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A Semi-Quadratic Buck-Boost Converter with Two Operating Modes and a Sustained Input-Output Current for PV Applications

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ABSTRACT

This study introduces a non-isolated semi-quadratic DC/DC buck-boost converter designed to enhance performance. Derived from a conventional CUK converter, the proposed topology operates in two distinct modes: one providing a semi-quadratic voltage gain of $D(2-D)/(1-D)^2$ and the other offering a gain of $D/(1-D)$. In addition, the proposed structure features constant input and output currents due to the presence of inductive filters at the input and output ports, which reduces the current stress on the capacitors at the output port and lowers the voltage ripple. Under steady-state conditions, the continuous conduction mode efficiency of the converter and small-signal modeling were analyzed by considering the effects of parasitic resistance. The results demonstrated lower total switching device power and a reduced component count than other buck-boost converters in dual-mode operation. The proposed converter was simulated using PLECS software. The experimental results were consistent with theoretical predictions due to their high efficiency and applications, particularly in photovoltaic systems and fuel cells.

I. Introduction

Fuel cells and photovoltaic (PV) systems are two examples of renewable energy (RE) sources that have recently received much attention as cost-effective solutions for electrical energy in domestic and industrial settings. The range of suitable energy transmission systems is constrained because these RE sources produce power with varying current and voltage magnitudes. For instance, their voltage needs to be raised when these sources are integrated into the grid to regulate energy flow. Similarly, it is crucial to lower the converter output voltage when using it as an energy source for particular appliances to prevent overvoltage damage [1]- [4]. Due to their intermittent nature and lower output voltage, PV panels must be equipped with an effective and reliable step-up DC-DC converter to ensure their output voltage meets the minimum requirements of power grid consumers. Studies presented various high-gain DC/DC converters to satisfy these requirements [5], [6]. Also, non-isolated traditional DC-DC converters were investigated [7], [8]. These sources also recognized the limitations imposed by traditional DC/DC converters and examined their efficiency in RE systems. Many buck-boost DC-DC converter designs have been presented based on conventional DC-DC converters, including boost, buck-boost, buck, SEPIC, ZETA, and CUK converters [9], [10]. Among the applications of a high-voltage gain converters is as a solar power optimizer (SPO) [11]-[13], a high-gain step-up/down converter to enhance the power delivery of a PV system to the grid. At the same time, it can be used as a buck-boost converter to charge DC batteries and sensitive DC loads. Among various types of converters used as SPO, the non-isolated converter topology has no isolation between the output and input sides. Thus, changes on the input side can directly affect the output. However, it has a lower component count than the isolated converter topology [14]. Other issues associated with this type of converter include poor voltage gain, high duty ratio, and more circuitry for optimal operations. In a study, a comprehensive analysis of various converter configurations was conducted through mathematical modeling to achieve a complete understanding of the dynamic

behavior of the converters [15]. Related research provided a unique step-up/down DC converter by considering the KY design [16] to accomplish a steady output current across two power switches. It is crucial to note that this converter has a relatively low voltage gain ratio. The SEPIC converters were designed with various components to enhance voltage gain and reduce voltage stress on the primary switch [17]. However, a multi-output system that requires such a converter necessitates complex control. To increase the voltage gain, a unique quadratic buck-boost converter with two power switches, each requiring a separate gate driver, was suggested [18]. Moreover, the drawback of having discontinuous input and output currents makes the control system more complicated [18, 19]. To overcome these challenges, quadratic buck-boost converters with continuous input current and lower voltage gain have been introduced [20, 21]. A ZETA converter with double the voltage gain is shown in [22] to attain better voltage gains with the constant input current. A single switch converter with continuous input/output current, and an odd ground between the input and output is provided in [23] for the same purpose. Similar to the previous study, a new step-up buck-boost converter was recommended [24, 25] to increase gain while reducing stress across the primary switch. However, this converter increases the voltage strains across the diodes. To improve performance, a unique buck-boost converter with inductive filters at the input/output ports and lower switching stress was introduced [26]. Nevertheless, this converter has more semiconductor components than other comparable architectures. The discontinuity problem is addressed in [27] by a quadratic DC/DC buck-boost topology with a low component count and constant input/output current, but at the expense of the voltage gain ratio. In various studies, novel quadratic transformerless DC/DC converters with negative output have been introduced [28, 29]. The structure had constant input and output currents due to employment of inductive filters at the input and output ports. A new high-gain SEPIC-based converter is proposed for renewable energy applications. The circuit is developed by merging a standard SEPIC topology with a boosting unit to increase voltage gain [30]. Similar topologies were described in [31] and [32], where the output current is discontinuous, despite improved performance in both boosting and bucking modes. In a similar study [33], researchers described a DC-DC converter with a positive output and lower overall switching device power throughout two modes of operation. Two operating modes are a step-up mode and a step-up/down mode with a high gain ratio. To achieve this, several boosting approaches were investigated, such as including the use of voltage multipliers, switched inductors, magnetic coupling switched capacitors, and multistage techniques [34]. These techniques are used in several high-gain DC-DC converters.

The CUK and buck-boost converters are traditional negative output (NO) converters. However, due to their limitations, a new NO buck-boost converter was proposed using a combination of buck-boost and conventional boost converters [35]. However, the negative and discontinuous output voltage causes high stress across one of the switches. Another NO converter with a wide conversion ratio is suggested in [36]. Nonetheless, it suffered from sporadic input/output current. The NO polarity is key in industrial applications, including data transfer interfaces and wind and solar power generation. In the dual-mode converters category, a new transformer-less inverter was also presented and prototyped [37]. In this single-phase inverter, various voltage gain ratios can be obtained to solve the deficiencies of modern dual-mode inverters. The dual-mode time-sharing approach effectively reduces unwanted high-frequency switching losses by determining when to apply the DC or the inverter stage during each grid voltage period [10]. Based on this technique, the converter's step-up mode operates only when the level of PV voltage is lower than the instantaneous level of the grid voltage, and the step-down mode operates when the PV voltage level is higher than the instantaneous level of the grid voltage. As a result, the dual-mode converters are even more effective than the classical two-stage grid-tied transformerless converters.

Fig. 1 represents the application of solar PV systems in dual-mode buck-boost converters. A novel coupled-inductor buck-boost converter with a simple design and two cascading semi-stages is presented in a related work [38]. This converter's key features include a constant input current with minimal ripple, adjustable output voltage, ultra-extended output voltage, and a positive polarity of the common ground. The converter's quadratic gain enables it to outperform traditional buck-boost converters in terms of step-down and step-up characteristics whenever the duty cycle is greater or less than 50%, respectively [39]. The proposed converter's unique current consistency between input and output decreases the current stress on the input and filtration capacitors, making it an attractive choice for renewable energy applications. In the event of a power switch open-circuit malfunction, three different quadratic buck DC-DC converter schemes were presented, each with the ability to flip to a semi-quadratic buck-boost configuration. A topological structure was established to ensure a secure transition from one switch to another while preserving the functional contribution of all other components to achieve efficient power conversion [40]. A new fifth-order boost converter was proposed for dual operating modes, utilizing different control methods. This converter's dual modes also show lower switch voltage stress [41]. The design of two cascaded buck-boost nature converters is completed; the first converter can produce high step-up gains, while the second can provide high step-down gains. Applications such as LED systems, which are voltage-sensitive, can benefit from this feature [42]. A new transformerless DC-DC converter with continuous input current for photovoltaic applications is presented. By optimizing the turns ratio of the coupled inductor, the converter enhances voltage gain and minimizes its overall size. This design also helps lower voltage stress on switching components. Furthermore, using one power switch simplifies control circuitry and reduces costs [43]. A new transformerless high step-up DC/DC converter with low input current ripple for renewable energy systems is proposed. The topology is built upon a conventional quadratic boost converter integrated with a CUK circuit, preserving key advantages such as continuous input and output currents. To achieve enhanced voltage gain, the design incorporates switched capacitors and switched-inductor techniques [44]. This paper presents a comprehensive study and analysis of a novel non-isolated high step-up DC-DC converter based on a SEPIC topology for photovoltaic applications. Derived from the conventional SEPIC converter, the proposed structure incorporates a two-winding coupled inductor

and an enhanced voltage multiplier cell to achieve an elevated voltage conversion ratio. This design approach enables the use of switches with lower on-state resistance, improving overall efficiency [45]. A novel high step-up DC-DC switched-mode converter featuring a shared ground connection between the input and output ports is introduced. Additionally, the converter prolongs the input source's service life by ensuring continuous current injection. The design also provides a fast dynamic response, achieved through its minimum-phase characteristics [46].

The CUK converter is the only common converter that achieves continuous output and input current with a smaller number of elements and flexible output, as mentioned before. Therefore, it is widely used for various applications. Studies showed that larger inductors with higher switching frequencies can minimize the input current ripple problem. However, bulky filters result in higher costs, larger sizes, and increased switching losses. To overcome these drawbacks, a novel DC/DC converter topology with low input current ripple and reduced filtering is developed in this study. This topology is based on a typical CUK converter. The proposed converter duty ratio provides a solution for controlling input current ripple in PV applications, achieving maximum overall efficiency without the need for a coupling inductor. The suggested converter features a wide range of conversion ratios, a buck-boost technique with two operating modes, and continuous input and output current in both buck and boost modes. Continuous input current (CIC) and continuous output current (COC) can be discussed in terms of their applications. For instance, CIC is an essential element in both PV and FC applications.

Regarding PV, CIC will increase energy extraction by reducing ripple power losses [44]; alternatively, in terms of FC, CIC will extend the lifetime of the FC stack by operating at nominal operating points. The COC feature, on the other hand, can reduce the size of the output capacitor while extending the battery's lifetime when used in charging applications. Due to its benefits, RE applications can significantly benefit from it.

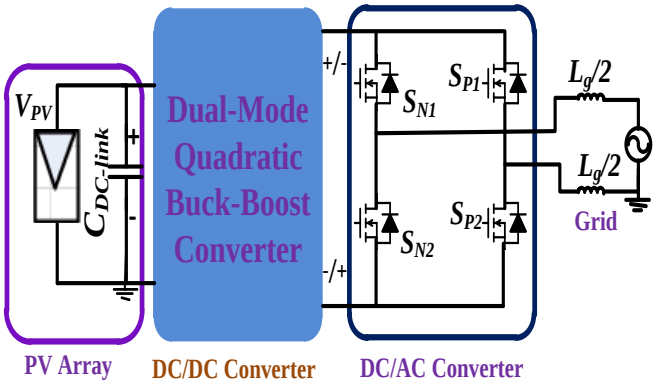


Fig. 1. Grid connected PV system through dual mode DC-DC converter.

The remainder of the paper is structured as follows. The suggested converter is introduced in Section 2 after theoretical analysis and steady-state validation. The evaluation of the small-signal modeling is presented in Section 3. The advantages of the suggested topology in comparison to other comparable conventional converters are covered in Section 4. The outcomes of the PLECS simulation are shown in Section 5. To support the theoretical arguments, Section 6 also offers the outcomes of the experimental prototype of the recommended converter. Lastly, Section 7 concludes.

II. Proposed Topology, Operation Principles, And Steady-State Evaluation

A. Proposed Topology

Constant input/output current port, cost-effectiveness, high efficiency, low noise and low input/output ripple currents are the most important characteristics of DC/DC semi quadratic buck-boost converter used in photovoltaic applications. Fig. 2 depicts the proposed semi-quadratic DC/DC buck-boost converter. The high-voltage gain proposed topology is made up of three inductors (L_1, L_2, L_3), three capacitors (C_1, C_2, C_o), two switches (S_1, S_2), two diodes (D_1, D_2), and a resistive load (R_o). The steady-state analysis of the suggested topology can be simplified by first considering the ideal components and then assuming all large enough capacitors to keep voltages virtually constant. As a result, their current and voltage were assumed to be constant across the whole duration. Fig. 3 depicts the proposed structure's distinctive waveforms.

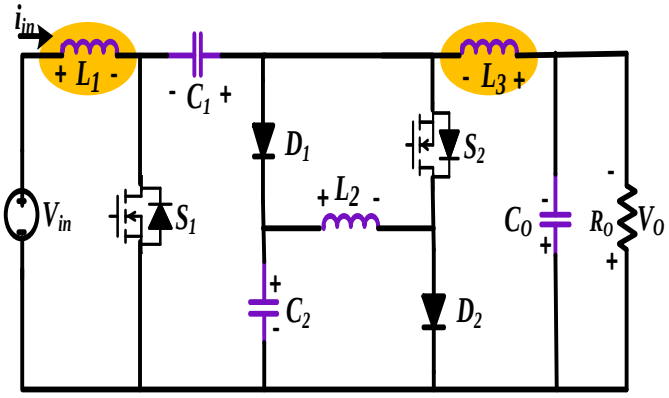


Fig. 2. The suggested converter's structure.

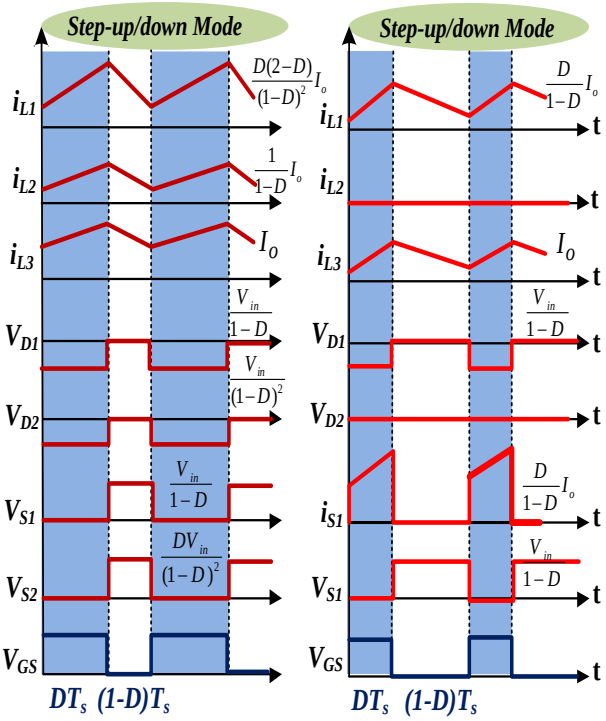


Fig. 3. The suggested structure's waveform characteristics for step-up/down mode.

B. Operation Principles of Proposed Topology

The steady-state conditions and continuous conduction mode (CCM) are taken into account while determining the features of the suggested converter. Thus, the consistent current and voltage are considered over a complete switching duration. As seen in Figs. 4 and 5, two major operating modes for the converter in the CCM are assumed.

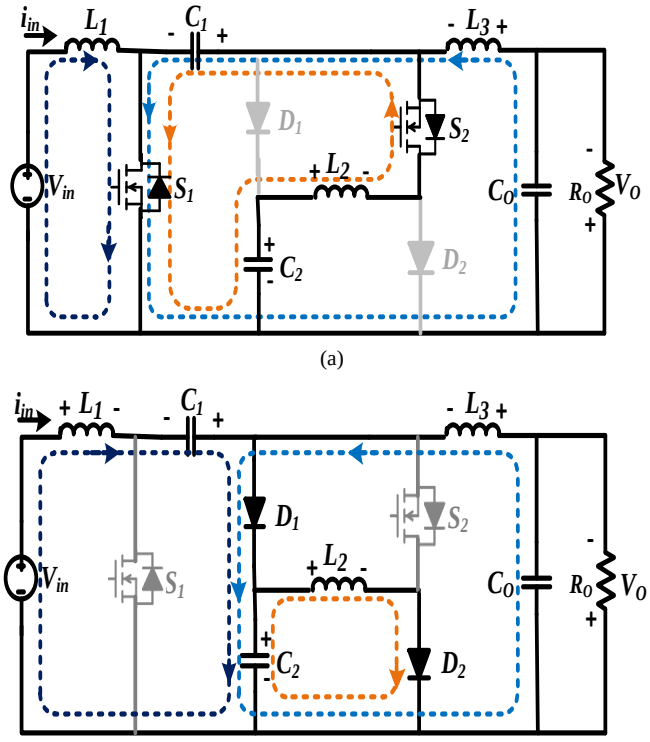


Fig. 4. The proposed converter's operational states for step-up mode (Mode I). (a) State 1; (b) State 2.

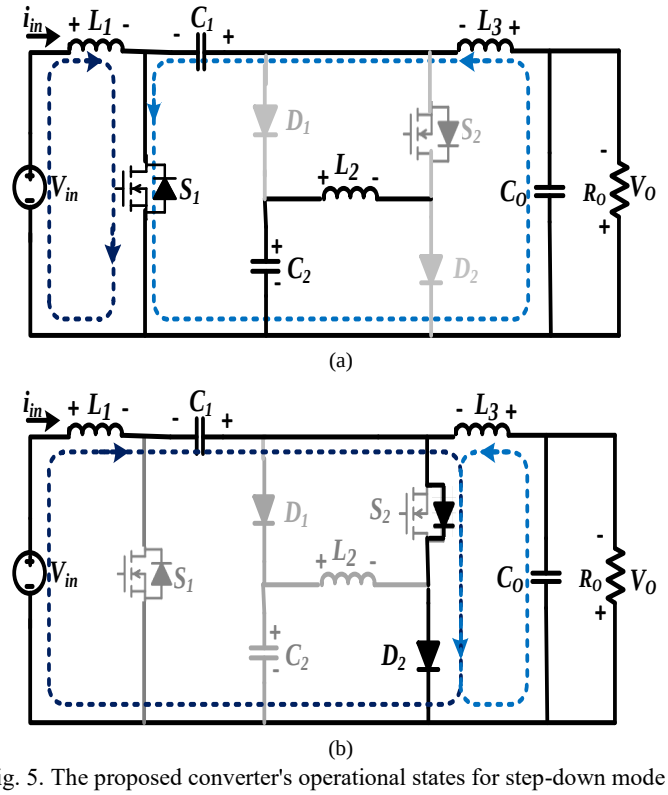


Fig. 5. The proposed converter's operational states for step-down mode (Mode II). (a) State 1; (b) State 2.

1) MODE I OPERATION

State 1 ($0 \le t \le DT$): The circuit is in this condition makes the power MOSFETs S_1 and S_2 are turned on and two diodes D_1 and D_2 are in reverse-biased mode as shown in Fig.4a. The inductors L_1, L_2, and L_3 are powered by the capacitor C_1 and the input source V_{in}. The capacitors C_1 and C_2 are discharged in this condition, and the current of the inductors (i_{L1}, i_{L2}, i_{L3}) rises. The output capacitor C_o supplies power to the output load R_o as seen in Fig.4a. The following relationships may be found using the KCL and KVL:

$$\begin{cases} V_{L1} = V_{in},\ V_{L2} = -V_{C1} + V_{C2},\ V_{L3} = -V_{C1} - V_o \\ i_{C1} = i_{L3} + i_{L2},\ i_{C2} = -i_{L2},\ i_{Co} = i_{L3} - \left({}^{V_o}/_{R_o}\right) \end{cases} \quad (1)$$

State 2 (DTs ≤ t ≤ Ts): Both power MOSFETs are switched off in this state. The diodes D1 and D2 are forward biased, and the inductors L1, L2, and L3 are de-energized as shown in Fig.4b. Here, the capacitor C1 and the capacitor C2 are charged. Moreover, inductor L3 feeds the output load Ro and also charges Co. Energy is discharged from capacitor C1 via the current paths of diodes D1 and D2. In this condition, the current and voltage equations are expressed as:

$$\begin{cases} V_{L1} = V_{in} + V_{C1} - V_{C2},\ V_{L2} = V_{C2},\ V_{L3} = -V_{C2} - V_o \\ i_{C1} = -i_{L1},\ i_{C2} = i_{L1} - i_{L2} + i_{L3},\ i_{Co} = i_{L3} - \left({}^{V_o}/_{R_o}\right) \end{cases} \quad (2)$$

2) MODE II OPERATION

State 1 ($0 \le t \le DT_s$): The power MOSFETs S_1 and S_2 are turned on and off during this period. Yet, diodes D_1 and D_2 are reverse-biased and forward-biased. The inductor L_1 is energized here by the input source, whereas L_2 is de-energized. The output capacitor C_o supplies power to the output load R_o. The equations relating to this period are calculated using the circuit depicted in Fig. 5a:

$$\begin{cases} V_{L1} = V_{in}, V_{L2} = 0, V_{L3} = -V_{C1} - V_o \\ i_{C1} = i_{L3},\ i_{C2} = -i_{L2} = 0,\ i_{Co} = i_{L3} - \left({}^{V_o}/_{R_o}\right) \end{cases} \quad (3)$$

State 2 ($DT_s \le t \le T_s$): In this condition, the power MOSFETs are switched off while diode D_1 is reverse-biased whereas diode D_2 is conducting. At this time frame, the capacitors C_1 and C_o are charged by releasing the stored energy in inductors L_1 and L_3, whereas L_2 is de-energized. Moreover, C_o is charged, and inductor L_3 supplies the output load R_o. As illustrated in Fig. 5b, the energy from all capacitors is discharged through the current route of the diode D_2, raising the current of each inductor. The voltage and current equations for this state, as represented by the KCL and KVL, are as follows:

$$\begin{cases} V_{L1} = V_{in} + V_{C1},\ V_{L2} = 0,\ V_{L3} = -V_o \\ i_{C1} = -i_{L1},\ i_{C2} = -i_{L2} = 0,\ i_{Co} = i_{L3} - \left({}^{V_o}/_{R_o}\right) \end{cases} \quad (4)$$

C. Steady-State Evaluation

This section derives the gain ratios and voltage and current relationships of the introduced converter shown in Figs. 4 and 5 (Mode I and II). Using the volt-second balance principle of inductors L_1, L_2, and L_3, the mean voltage value of all capacitors throughout the charge-discharge period can be calculated. Using D as the duty

cycle, the average voltages of capacitors C_1 and C_2 may thus be represented as:

$$\begin{cases} Mode\ I:\ V_{C1}=\dfrac{1}{(1-D)^2}V_{in},\ \ V_{C2}=\dfrac{D}{(1-D)^2}V_{in} \\ Mode\ II:\ V_{C1}=\dfrac{1}{1-D}V_{in},\ \ V_{C2}=0 \end{cases} \quad (5)$$

Therefore, the voltage gains are expressed as,

$$\begin{cases} Mode\ I:\ M_{CCM}=\left(\dfrac{V_o}{V_{in}}\right)=\dfrac{D(2-D)}{(1-D)^2} \\ Mode\ II:\ M_{CCM}=\left(\dfrac{V_o}{V_{in}}\right)=\dfrac{D}{(1-D)} \end{cases} \quad (6)$$

Assuming negligible circuit losses, it is possible to consider the input power along with output power as follows:

$$P_{in}=P_o \rightarrow V_{in}I_{in}=V_oI_o \quad (7)$$

The relationship between DC output current and DC input current can be expressed by, using the voltage gain calculated in (6) as follows:

$$\begin{cases} Mode\ I:\ \dfrac{I_o}{I_{in}}=\dfrac{(1-D)^2}{D(2-D)} \\ Mode\ II:\ \dfrac{I_o}{I_{in}}=\dfrac{(1-D)}{D} \end{cases} \quad (8)$$

Using the ampere-second balancing concept of capacitors C_1, C_2, and C_o, the average magnitude for every inductor current can be provided as:

$$\begin{cases} Mode\ I:\ I_{LI}=\dfrac{D(2-D)}{(1-D)^2}|I_o|,\ \ I_{L2}=\dfrac{|I_o|}{1-D},\ \ I_{L3}=|I_o| \\ Mode\ II:\ I_{LI}=\dfrac{D}{(1-D)}|I_o|,\ \ I_{L2}=0,\ \ I_{L3}=|I_o| \end{cases} \quad (9)$$

Then the current and voltage stress of the two diodes and two power MOSFETs can be calculated as follows:

$$\begin{cases} Mode\ I:\ V_{S1}=\dfrac{1}{1-D}V_{in},\ \ V_{S2}=\dfrac{D}{(1-D)^2}V_{in} \\ Mode\ II:\ V_{s1,2}=\dfrac{1}{1-D}V_{in} \end{cases} \quad (10)$$

$$\begin{cases} Mode\ I:\ I_{S1-avg}=\dfrac{D(2-D)}{(1-D)^2}|I_o|,\ \ I_{S2-avg}=\dfrac{D}{1-D}|I_o| \\ Mode\ II:\ I_{S1-avg}=\dfrac{D}{1-D}|I_o|,\ \ I_{S2-avg}=|I_o| \end{cases} \quad (11)$$

$$\begin{cases} Mode\ I:\ V_{D1}=\dfrac{1}{1-D}V_{in},\ \ V_{D2}=\dfrac{1}{(1-D)^2}V_{in} \\ Mode\ II:\ V_{D1}=\dfrac{1}{1-D}V_{in},\ \ V_{D2}=0 \end{cases} \quad (12)$$

$$\begin{cases} Mode\ I:\ I_{D1-avg}=\dfrac{1}{1-D}|I_o|,\ \ I_{D2-avg}=|I_o| \\ Mode\ II:\ I_{D1-avg}=0,\ \ I_{D2-avg}=|I_o| \end{cases} \quad (13)$$

D. Efficiency Inspection

The power loss in the proposed converter circuit is affected by several parameters, including the internal resistances of the converter's elements, the forward voltage drops of the diode, and the switching frequency. The circuit shown in Fig. 6 is utilized to compute the amount of loss in each circuit element.

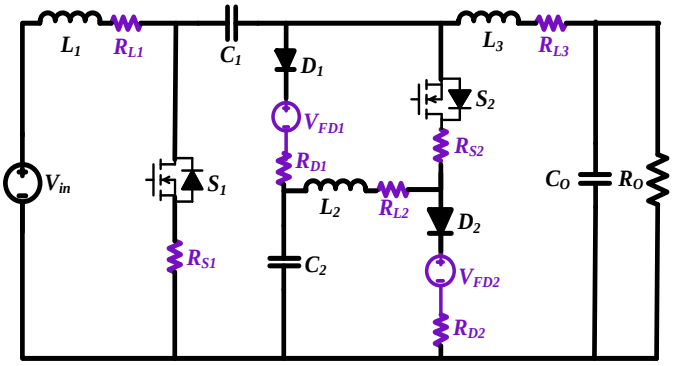


Fig. 6. The analogous circuit with parasitic components.

Currents flowing through switches and diodes are approximated using the following RMS values as follows:

$$I_{S1-RMS}\approx\frac{(2-D)\sqrt{D}}{(1-D)^2}|I_o|, I_{S2-RMS}=\frac{\sqrt{D}}{1-D}|I_o| \quad (14)$$

$$I_{D1-RMS}=\frac{I_o}{\sqrt{(1-D)^3}}, I_{D2-RMS}=\frac{I_o}{\sqrt{(1-D)}} \quad (15)$$

Moreover, the following equations are used to calculate the estimated RMS values of currents flowing between the inductors and capacitors:

$$I_{L1-RMS}\approx\frac{D(2-D)I_o}{(1-D)^2}, I_{L2-RMS}\approx\frac{I_o}{1-D}, I_{L3-RMS}\approx I_o \quad (16)$$

$$I_{C1-RMS}\approx\sqrt{\frac{D(2-D)}{(1-D)^3}}I_o, I_{C2-RMS}\approx\sqrt{\frac{D}{(1-D)^3}}I_o, \quad I_{C3-RMS}\approx 0 \quad (17)$$

Power switch total power loss ($P_{S1,2\text{-}Total}$) is defined as the switching losses ($P_{S\text{-}L}$) and sum of conducting power dissipations ($P_{R\text{-}S}$). Using the R_S value as the power switch's conduction resistance, one may derive:

$$P_{S1,2-Total}=P_{s-L}+P_{R-S} \quad (18)$$

$$\begin{cases} P_{R-S1}=R_{S1}I_{S1-RMS}^2=R_{S1}\dfrac{(2-D)^4}{(1-D)^4}I_o^2 \\ P_{R-S2}=R_{S2}I_{S2-RMS}^2=R_{S2}\dfrac{D}{(1-D)^2}I_o^2 \\ P_{S1-L}=f_sC_{S1}V_{S1}^2=f_sC_{S1}\dfrac{1}{(1-D)^2}V_{in}^2 \\ P_{S2-L}=f_sC_{S2}V_{S2}^2=f_sC_{S2}\dfrac{D^2}{(1-D)^4}V_{in}^2 \end{cases} \quad (19)$$

Additionally, diode forward conduction resistance (R_{FD}) and forward bias voltage (V_{FD}) are used to calculate total diode losses ($P_{FD}+P_{FR}$), where P_{FD} signifies forward bias losses and P_{FR} denotes reverse bias losses, respectively.

$$P_{D-Total}=P_{FD}+P_{FR}=\sum_{i=1}^{2}(R_{FD}I_{Di-RMS}^2)+\sum_{i=1}^{2}(V_{FDi}I_{Di}) \quad (20)$$

Using the equivalent series resistance (ESR) values (R_L and R_C) of inductors and capacitors, as well as their power losses, may be computed as:

$$P_{L-Total}=\sum_{i=1}^{3}(P_{Li})=\sum_{i=1}^{3}(R_{Li}I_{Li-RMS}^2) \quad (21)$$

$$P_{C-Total}=P_{C1}+P_{C2}+P_{Co} \quad (22)$$

The proposed converter's overall power losses are the sum of the power losses of capacitors, inductors, diodes, and power MOSFETs, as shown below:

$$P_{loss-Total} = P_{s-Total} + P_{D-Total} + P_{L-Total} + P_{C-Total} \quad (23)$$

Eventually, the proposed converter's efficiency may be derived as:

$$\eta = \frac{P_o}{P_{loss-Total} + P_o} = \frac{1}{\frac{P_{loss-Total}}{RI_o^2} + 1} \quad (24)$$

1) Circuit Simplification with Parasitic Parameters

Fig.6 depicts a simplified circuit with parasitic components, including parasitic parameters of inductors (L_1, L_2, and L_3), diodes (D_1 and D_2), and MOSFETs (S_1 and S_2). V_{FD1} and V_{FD2} are the threshold voltages of diodes. Then, as shown below, the inductor voltage equations with parasitic parameters (R_{S1}, R_{S2}, R_{D1}, R_{D2}, R_{L1}, R_{L2}, R_{L3}) can be determined.

For the two operation states (Mode I), the voltages across the inductors with parasitic parameters are determined as follows:

$$State\ 1: \begin{cases} V_{L1} = V_{in} - R_{L1}I_{L1} - R_{S1}I_{S1} = V_{in} - \\ R_{L1}\frac{D^2(2-D)^2}{(1-D)^4}\frac{V_{in}}{R_o} - R_{s1}\frac{D^2(2-D)^2}{(1-D)^4}\frac{V_{in}}{R_o} \\ V_{L2} = -R_{L2}I_{L2} - R_{S1}I_{S1} - R_{S2}I_{S2} - V_{C1} + V_{C2} \\ = -R_{L2}\frac{D(2-D)}{(1-D)^3}\frac{V_{in}}{R_o} - R_{s1}\frac{D^2(2-D)^2}{(1-D)^4}\frac{V_{in}}{R_o} \\ -R_{s2}\frac{D^2(2-D)^2}{(1-D)^3}\frac{V_{in}}{R_o} - V_{C1} + V_{C2} \\ V_{L3} = -R_{L3}I_{L3} - R_{S1}I_{S1} - V_{C1} - V_o = \\ -R_{L3}\frac{D(2-D)}{(1-D)^2}\frac{V_{in}}{R_o} - R_{s1}\frac{D^2(2-D)^2}{(1-D)^4}\frac{V_{in}}{R_o} - \\ V_{C1} - V_o \end{cases} \quad (25)$$

$$State\ 2: \begin{cases} V_{L1} = V_{in} - R_{L1}I_{L1} - R_{D1}I_{D1} + V_{C1} - V_{C2} - \\ V_{FD1} = V_{in} - R_{L1}\frac{D^2(2-D)^2}{(1-D)^4}\frac{V_{in}}{R_o} - \\ R_{D1}\frac{D(2-D)}{(1-D)^3}\frac{V_{in}}{R_o} + V_{C1} - V_{C2} - V_{FD1} \\ V_{L2} = -R_{L2}I_{L2} - R_{D2}I_{D2} + V_{C2} - V_{FD2} \\ = -R_{L2}\frac{D(2-D)}{(1-D)^3}\frac{V_{in}}{R_o} - R_{D2}\frac{D(2-D)}{(1-D)^2}\frac{V_{in}}{R_o} + \\ V_{C2} - V_{FD2} \\ V_{L3} = -R_{L3}I_{L3} - R_{D1}I_{D1} - V_{C2} - V_{FD1} - \\ V_o = -R_{L3}\frac{D(2-D)}{(1-D)^2}\frac{V_{in}}{R_o} + R_{D1}\frac{D(2-D)}{(1-D)^3}\frac{V_{in}}{R_o} - \\ V_{C2} - V_{FD1} - V_o \end{cases} \quad (26)$$

Using the voltage-second balancing concept of inductors one can yield the voltage gain with parasitic elements. As a consequence, the average capacitor voltages C_1 and C_2 and the voltage gain ratio with parasitic characteristics can be expressed as:

$$V_{C1} = \frac{\begin{array}{c} -(1-D)^4R_oV_{in} + D^2(2-D)^2R_{L1}V_{in} + \\ D(2-D)(1-D)^3R_{L2}V_{in} + \\ D^3(2-D)^2R_{S1}V_{in} + D^3(2-D)(1-D)^2R_{S2}V_{in} + \\ D(2-D)(1-D)^2R_{D1}V_{in} + D(2-D)(1-D)^4R_{D2}V_{in} + \\ (1-D)^5R_oV_{FD1} - (1-D)^6R_oV_{FD2} \end{array}}{(1-D)^6R_o} \quad (27)$$

$$V_{C2} = \frac{\begin{array}{c} -D(1-D)^4R_oV_{in} + D^3(2-D)^2R_{L1}V_{in} + \\ D(2-D)(1-D)^3R_{L2}V_{in} + D^4(2-D)^2R_{S1}V_{in} + \\ D^3(2-D)(1-D)^2R_{S2}V_{in} + D^2(2-D)(1-D)^2R_{D1}V_{in} \\ +D(2-D)(1-D)^4R_{D2}V_{in} + D(1-D)^5R_oV_{FD1} + \\ (1-D)^6R_oV_{FD2} \end{array}}{(1-D)^6R_o} \quad (28)$$

$$M = \frac{V_o}{V_{in}} = \frac{\begin{array}{c} D(2-D)(1-D)^4R_o - D^3(2-D)^3R_{L1} - D(2-D)(1-D)^3R_{L2} \\ -D(2-D)(1-D)^4R_{L3} + D^3(2-D)^2R_{S1} - D^3(2-D)(1-D)^2R_{S2} \\ -D(2-D)(1-D)^2R_{D1} - D(2-D)(1-D)^4R_{D2} - \\ (1-D)^5R_o\frac{V_{FD1}}{V_{in}} - (1-D)^6R_o\frac{V_{FD2}}{V_{in}} \end{array}}{(1-D)^6R_o} \quad (29)$$

Likewise, by employing the volt-second balance principle of inductors, the mean output voltage can be determined while taking into consideration the presence of parasitic elements:

$$V_o = \frac{D(2-D)(1-D)^4V_{in} - (1-D)^6V_{FD_2} - (1-D)^5V_{FD_1}}{(1-D)^6 + \alpha_1\frac{R_{L1}}{R_o} + \alpha_2\frac{R_{L2}}{R_o} + \alpha_3\frac{R_{L3}}{R_o} + \alpha_4\frac{R_{S1}}{R_o} + \alpha_5\frac{R_{S2}}{R_o} + \alpha_6\frac{R_{D1}}{R_o} + \alpha_7\frac{R_{D2}}{R_o}}$$

$$\alpha_1 = D^2(2-D)^2(1-D)^2, \alpha_2 = (1-D)^5, \alpha_3 = (1-D)^6, \alpha_4 = D^2(2-D)(1-D)^2, \alpha_5 = D^2(1-D)^4, \alpha_6 = (1-D)^4, \alpha_7 = (1-D)^6 \quad (30)$$

The plots presented in Fig.7 demonstrate that the voltage gain ratio $|M_{CCM}|$ is influenced by parasitic resistance R_L along with the forward drop in voltage of diode V_{FD}.

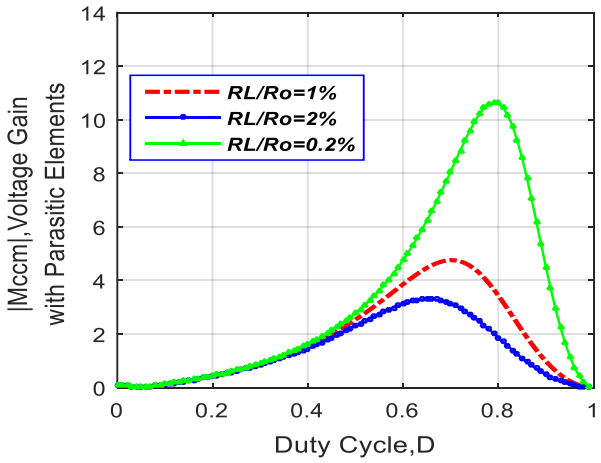
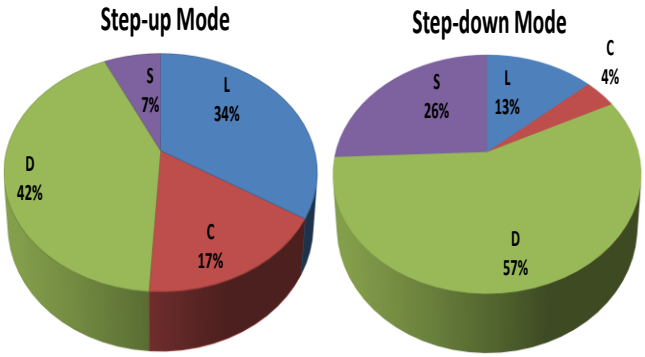


Fig. 7. |MCCM| with the parasitic resistance versus duty cycle (Mode I).

These points out those parasitic components have an effect on the voltage gain ratio. Hence, Vin=15V, $V_{FD1,2}$=0.8V and $R_{L1,2,3}$ =Δ×Ro, where Δ=1%, 2%, 0.2%.

2) Proportion of Power Losses

Fig.8 illustrates the power loss distribution in Mode I, aiding in the understanding of the power losses of individual element sections. The step-down state exhibits lower efficiency compared to the step-up state. The converter operates in step-up mode whereby the input current is greater than the expected output current of the converter. In the step-down mode of operation, it is observed that the current flowing through the input port is lesser than the current flowing through the output port. As a result, as compared to the step-up mode, the step-down mode has a lower overall efficiency. In step-up/down mode, the power losses of inductors (*L*), capacitors (*C*), power MOSFETs (*S*), and diodes (*D*), and are given in (21), (22), (18), and (20).



(a) (b)

Fig. 8. Power loss distribution for mode I. (a) Step-up mode, (b) Step-down mode.

E. Analysis and Design of Inductor

This section describes the detail design requirements of inductors used in the converter.

1) Inductor Ripples

The value of ripple of inductor currents i_{L1}, i_{L2}, and i_{L3} can be calculated using circuit diagram shown in Fig. 4(a) as expressed below [9].

$$\Delta i_L = \frac{DV_L}{Lf_s} \tag{31}$$

Current ripples are taken into account when designing the inductors in the proposed converter. In relation to the peak-to-peak current displayed in Fig.4a, and assuming that current ripples inductors of (31), the needed inductances and ripples inductor currents as expressed below:

$$L = \frac{DV_L}{\alpha\%\Delta i_L f_s}, \qquad \Delta i_L \le \alpha\% i_L \ \ \alpha \le 30\% \tag{32}$$

Substituting $I_{L1,2,3}$ from (9) to (32), the following relation can be obtained:

$$L_1 \ge \frac{(1-D)^4}{\alpha\% D(2-D)^2} \times \frac{R_o}{f_s}, L_{2,3} \ge \frac{D(1-D)}{\alpha\%(2-D)} \times \frac{R_o}{f_s} \tag{33}$$

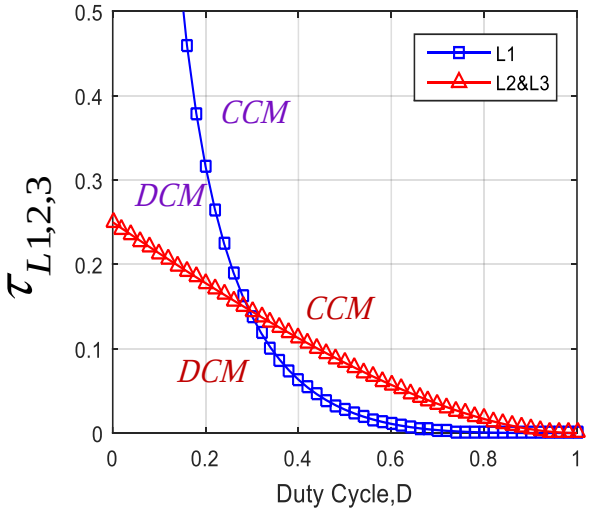
2) Boundary Calculation

The inductor current minimum value zero marks the border between CCM and DCM (discontinuous conduction mode). It is critical to build the discrete inductors in such a way that the given converter can operate in continuous conduction mode. Taking this into consideration, the CCM condition is found using the circuit shown in Figs.4a and 5a for inductors L_3, L_2, and L_1as follows:

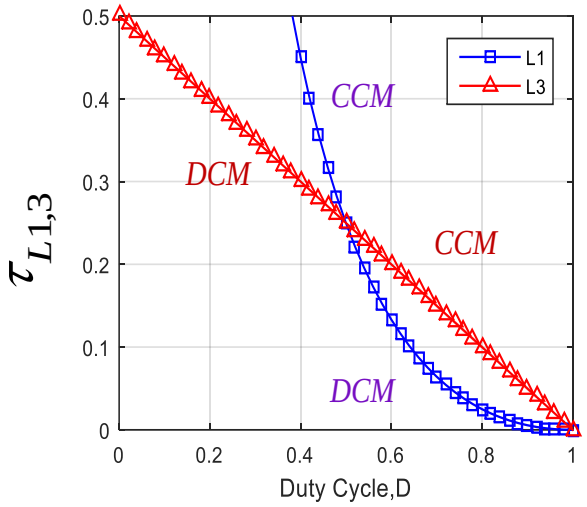
$$\begin{aligned} Mode\ I&: \begin{cases} L_1 \ge \dfrac{(1-D)^4}{D(2-D)^2} \times \dfrac{R_o}{f_s} \\ L_{2,3} \ge \dfrac{(1-D)^2}{(2-D)} \times \dfrac{R_o}{f_s} \end{cases}, \\ Mode\ II&: \begin{cases} L_1 \ge \dfrac{(1-D)^2}{D} \times \dfrac{R_o}{f_s} \\ L_3 \ge (1-D) \times \dfrac{R_o}{f_s} \end{cases} \end{aligned} \tag{34}$$

The boundary conditions (τ_{LB}) for L_3, L_2, and L_1 in Mode I and II are provided in the (35). The CCM is shown by the area above each curve in Fig.9, while the DCM is represented by the area below.

$$\begin{aligned} Mode\ I&: \begin{cases} \tau_{L1B} = \dfrac{(1-D)^4}{2D(2-D)^2} \\ \tau_{L2,3B} = \dfrac{(1-D)^2}{2(2-D)} \end{cases}, \\ Mode\ II&: \begin{cases} \tau_{L1B} = \dfrac{(1-D)^2}{2D} \\ \tau_{L3B} = \dfrac{(1-D)}{2} \end{cases} \end{aligned} \tag{35}$$



(a)



(b)

Fig. 9. Boundary conditions of Input and output current ripple versus duty cycle. (a) Mode I; (b) Mode II.

F. Capacitor Design and Analysis

The voltage ripples across capacitors C_1, C_2 and C_o may be represented as [9]:

$$\Delta V_{C1,2} = \frac{Di_{C1,2}}{C_{1,2}f_s}, \Delta V_{Co} = \frac{Di_{Co}}{C_o f_s} \tag{36}$$

Also, based on the following conditions, the capacitances of each capacitor can be obtained as:

$$\begin{cases} \Delta v_{C_{1,2}} \le \beta\% V_{C1,2} \quad \beta \le 2\% \\ \Delta v_{C_o} \le \delta\% V_o \quad \delta \le 0.5\% \end{cases} \tag{37}$$

$$\begin{cases} C_{1,2} = \dfrac{DI_{C1,2}}{\beta\% V_{C1,2} f_s} \\ C_o = \dfrac{DI_o}{\delta\% V_o f_s} \end{cases} \tag{38}$$

III. Small Signal Modeling

The equations required for small signal modelling for the dual states can be obtained from Figs. 4and 5, Following is a straightforward derivation of the state-average model using the averaging method and equations (39) and (40) for mode I and (41) and (42) for mode II [47], as below:

MODE I OPERATION

$$State1: \begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in} \\ L_2 \dfrac{di_{L2}}{dt} = -v_{C1} + v_{C2} \\ L_3 \dfrac{di_{L3}}{dt} = -v_{C1} - v_{Co} \\ C_1 \dfrac{dv_{C1}}{dt} = i_{L3} + i_{L2} \\ C_2 \dfrac{dv_{C2}}{dt} = i_{L2} \\ C_o \dfrac{dv_{Co}}{dt} = i_{L3} - \dfrac{v_{Co}}{R_o} \end{cases},$$

$$State\ 2: \begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in} + v_{C1} - v_{C2} \\ L_2 \dfrac{di_{L2}}{dt} = -v_{C2} \\ L_3 \dfrac{di_{L3}}{dt} = -v_{C2} - v_{Co} \\ C_1 \dfrac{dv_{C1}}{dt} = -i_{L1} \\ C_2 \dfrac{dv_{C2}}{dt} = i_{L1} - i_{L2} + i_{L3} \\ C_o \dfrac{dv_{Co}}{dt} = i_{L3} - \dfrac{v_{Co}}{R_o} \end{cases} \tag{39}$$

State1

$$\begin{cases} L_1 \dfrac{d\langle i_{L1}\rangle}{dt} = d(\langle v_{in}\rangle) + (1-d)(\langle v_{in}\rangle + \langle v_{C1}\rangle - \langle v_{C2}\rangle) \\ L_2 \dfrac{d\langle i_{L2}\rangle}{dt} = d(-\langle v_{C1}\rangle + \langle v_{C2}\rangle) - (1-d)\langle v_{C2}\rangle \\ L_3 \dfrac{d\langle i_{L3}\rangle}{dt} = -d(\langle v_{C1}\rangle + \langle v_{Co}\rangle) - (1-d)(\langle v_{C2}\rangle + \langle v_{Co}\rangle) \end{cases}$$

State2

$$\begin{cases} C_1 \dfrac{d\langle v_{C1}\rangle}{dt} = d(\langle i_{L3}\rangle + \langle i_{L2}\rangle) - (1-d)\langle i_{L1}\rangle \\ C_2 \dfrac{d\langle v_{C2}\rangle}{dt} = d(\langle i_{L2}\rangle) + (1-d)(\langle i_{L1}\rangle - \langle i_{L2}\rangle + \langle i_{L3}\rangle) \\ C_o \dfrac{d\langle v_{Co}\rangle}{dt} = d(\langle i_{L3}\rangle + \langle \dfrac{v_{Co}}{R_o}\rangle) - (1-d)(\langle i_{L3}\rangle + \langle \dfrac{v_{Co}}{R_o}\rangle) \end{cases} \tag{40}$$

MODE II OPERATION

$$State1: \begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in} \\ L_2 \dfrac{di_{L2}}{dt} = 0 \\ L_3 \dfrac{di_{L3}}{dt} = -v_{C1} - v_{Co} \\ C_1 \dfrac{dv_{C1}}{dt} = i_{L3} \\ C_2 \dfrac{dv_{C2}}{dt} = -i_{L2} = 0 \\ C_o \dfrac{dv_{Co}}{dt} = i_{L3} - \dfrac{v_{Co}}{R_o} \end{cases}, \tag{41}$$

$$State\ 2: \begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_{in} + v_{C1} \\ L_2 \dfrac{di_{L2}}{dt} = 0 \\ L_3 \dfrac{di_{L3}}{dt} = -v_{Co} \\ C_1 \dfrac{dv_{C1}}{dt} = -i_{L1} \\ C_2 \dfrac{dv_{C2}}{dt} = -i_{L2} = 0 \\ C_o \dfrac{dv_{Co}}{dt} = i_{L3} - \dfrac{v_{Co}}{R_o} \end{cases}$$

State1

$$\begin{cases} L_1\frac{d\langle i_{L1}\rangle}{dt} = d(\langle v_{in}\rangle) + (1-d)(\langle v_{in}\rangle + \langle v_{C1}\rangle) \\ L_2\frac{d\langle i_{L2}\rangle}{dt} = 0 \\ L_3\frac{d\langle i_{L3}\rangle}{dt} = -d(\langle v_{C1}\rangle + \langle v_{Co}\rangle) - (1-d)(-\langle v_{Co}\rangle) \end{cases}$$

State2 (42)

$$\begin{cases} C_1\frac{d\langle v_{C1}\rangle}{dt} = d(\langle i_{L3}\rangle) - (1-d)\langle i_{L1}\rangle \\ C_2\frac{d\langle v_{C2}\rangle}{dt} = 0 \\ C_o\frac{d\langle v_{Co}\rangle}{dt} = d(\langle i_{L3}\rangle + \langle\frac{v_{Co}}{R_o}\rangle) - (1-d)(\langle i_{L3}\rangle + \langle\frac{v_{Co}}{R_o}\rangle) \end{cases}$$

Where,$\langle v_{in}\rangle, \langle i_{L3}\rangle, \langle i_{L2}\rangle, \langle i_{L1}\rangle, \langle v_{C2}\rangle, \langle v_{C1}\rangle$ and $\langle v_{C0}\rangle$are the average values of v_{in}, , i_{L3}, i_{L2}, i_{L1}, v_{C2}, v_{C1}, and v_{Co}, and respectively. Small AC values of the aforementioned elements are specified in order to produce the small-signal model as: $\widehat{v_{in}}, \widehat{i_{L3}}, \widehat{i_{L2}}, \widehat{i_{L1}}, \widehat{v_{c2}}, \widehat{v_{c1}}, \widehat{v_{c0}}$, and $\hat{d}$. Besides, the associations among mean AC, and DC values can be expressed as:

$$\begin{cases} \langle v_{in}\rangle = V_{in} + \hat{v_{in}} \\ \langle v_{C1}\rangle = V_{C1} + \hat{v_{C1}} \\ \langle v_{C2}\rangle = V_{C2} + \hat{v_{C2}} \\ \langle v_{Co}\rangle = V_{Co} + \hat{v_{Co}} \\ \langle i_{L1}\rangle = I_{L1} + \hat{i_{L1}} \\ \langle i_{L2}\rangle = I_{L2} + \hat{i_{L2}} \\ \langle i_{L3}\rangle = I_{L3} + \hat{i_{L3}} \\ \langle d\rangle = D + \hat{d} \end{cases} \quad \begin{cases} |\hat{v_{in}}| \ll |V_{in}|, \\ |\hat{v_{C1}}| \ll |V_{C1}| \\ |\hat{v_{C2}}| \ll |V_{C2}| \\ |\hat{v_{Co}}| \ll |V_{Co}| \\ |\hat{i_{L1}}| \ll |I_{L1}| \\ |\hat{i_{L2}}| \ll |I_{L2}| \\ |\hat{i_{L3}}| \ll |I_{L3}| \\ |\hat{d}| \ll |D| \end{cases} \quad (43)$$

By substituting (43) into (42) and (40), one may get AC and DC values while omitting the high-order small signal components as:

$$K\dot{x} = Ax + Bu, y = Cx + Eu \quad (44)$$

with

$$x = [\widehat{i_{L1}} \quad \widehat{i_{L2}} \quad \widehat{i_{L3}} \quad \widehat{v_{C1}} \quad \widehat{v_{C2}} \quad \widehat{v_{Co}}], u = [\hat{d} \quad \widehat{v_{in}}] \quad (45)$$

$$K = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_2 & 0 & 0 & 0 & 0 \\ 0 & 0 & L_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & C_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & C_o \end{bmatrix} \quad (46)$$

$$A_{Mode\ I=} \begin{bmatrix} 0 & 0 & 0 & (1-D) & -(1-D) & 0 \\ 0 & 0 & 0 & -D & 1 & 0 \\ 0 & 0 & 0 & -D & -(1-D) & -1 \\ -(1-D) & D & D & 0 & 0 & 0 \\ (1-D) & -1 & -(1-D) & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -\frac{1}{R_O} \end{bmatrix}$$

$$A_{Mode\ II} = \begin{bmatrix} 0 & 0 & 0 & 0 & (1-D) & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -D & 0 & 0 \\ -(1-D) & 0 & D & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1/R_O \end{bmatrix} \quad (47)$$

$$B_{Mode\ I} = \begin{bmatrix} -V_{C1} + V_{C2} & 1 \\ -V_{C1} & 0 \\ -V_{C1} + V_{C2} & 0 \\ I_{L1} + I_{L2} + I_{L3} & 0 \\ -I_{L1} - I_{L3} & 0 \\ 0 & 0 \end{bmatrix}, B_{Mode\ II} = \begin{bmatrix} -V_{C1} & 1 \\ 0 & 0 \\ -V_{C1} & 0 \\ I_{L1} + I_{L3} & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad (48)$$

And the V_o metrics can be obtained as below:

$$V_o = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad 1]\begin{bmatrix} \hat{i_{L1}} \\ \hat{i_{L2}} \\ \hat{i_{L3}} \\ \hat{v_{C1}} \\ \hat{v_{C2}} \\ \hat{v_{Co}} \end{bmatrix} + [0 \quad 0]\begin{bmatrix} \hat{d} \\ \hat{V_{in}} \end{bmatrix} \quad (49)$$

The extracted bode plots from the calculation procedure and simulations are displayed in Fig 10. It is used to generate the output transfer function to test the model. The parameters listed in Table III are used to draw the bode diagrams. As can be seen, the estimated model and simulation results are in good agreement. As a result, the suggested model may be used to exact controller design as well as dynamic behavior of the circuit. Fig.11 illustrates the control system parameters using SISOTOOL in MATLAB, which are determined according to the gain and phase margin. The PI controller's step-up/step-down functionality allows for an output voltage range of 15V to 60V. However, modifying the load in an open-loop control system results in alterations to the output voltage ripples.

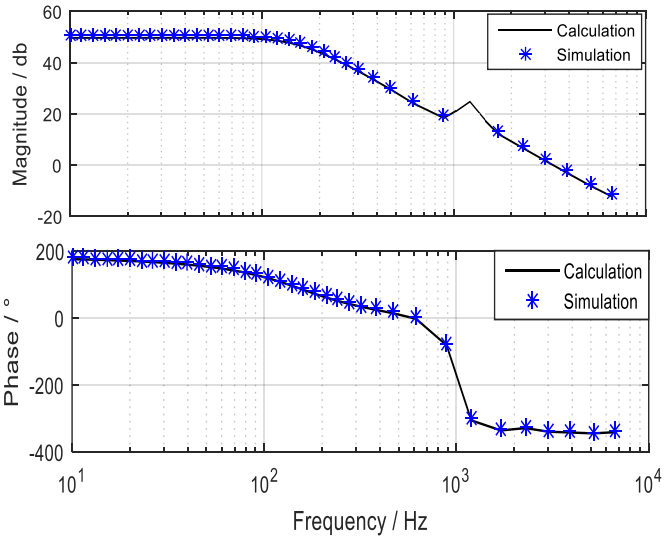


Fig. 10. Comparison of bode diagrams comparison the theoretical and simulation results.

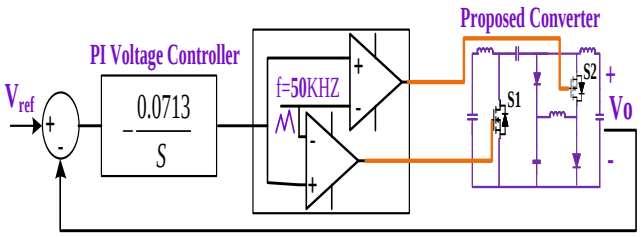


Fig. 11. PI controller system for the proposed

IV. Comparison with Existing Converters

The characteristics of modes I and II of the suggested converter in step-up/down modes is shown in Table I. Fig.12 depicts the buck and boost zones of modes I and II. To compare the suggested converter to similar dual-mode converters, converters in [36] and [37] are explored independently in Table I. The number of semiconductor components and voltage gain ratio of mode I are lower and greater, respectively, than in [37]. The SDP of the suggested topology is lower than [37], as shown in Table I, and the elements are fewer. While having eight elements, the converter in [36] has discontinuous output and input currents, unlike the proposed converter. Moreover, in step-up/down mode, the suggested converter has a lower switching device power (SDP) than [37]. As a result, the proposed converter has more advantage. Table II summarizes the characteristics of the suggested DC/DC buck-boost topology and existing converters.

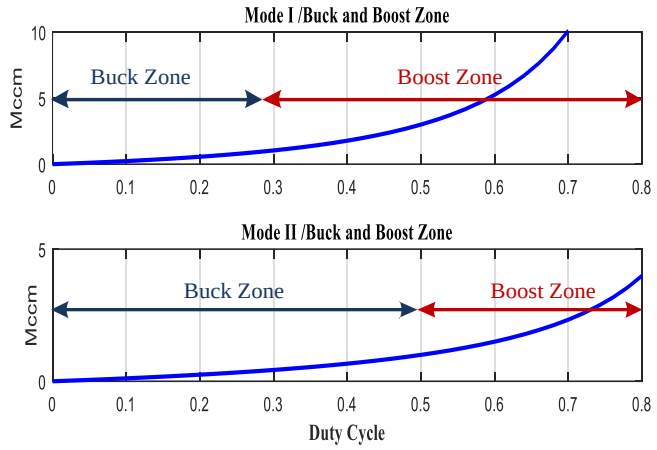


Fig. 12. Buck and Boost mode zone of modes I and II.

As shown in Table II, the number of semiconductor components, as well as the voltage stress of switches, voltage gain ratio, SDP_{avg}/P_o, output polarity, diode voltage stress, and continuous input/output current, were analyzed for the given converter and existing converters. Despite the suggested converter's continuous input current and correspondingly fewer semiconductor components, it may be a good solution for PV inverters. The suggested structure includes continuous input/output current. The subsequent section showcases the preeminence of the converter that has been recommended, with regard to voltage gain, effectiveness index, and SDP.

A. Voltage Gain Ratio Differences

Fig. 13 compares voltage gain ratios, and Table II contains statistics on the proposed and other competing converters. If D > 0.5, the investigated converter has a higher voltage gain than comparable converters. The horizontal axis, as displayed, represents the duty cycle (0 to 100%). Additionally, the vertical axis displays the output voltage in the 0-20V range. The higher the duty cycle, the higher the output voltage, but with more power loss.

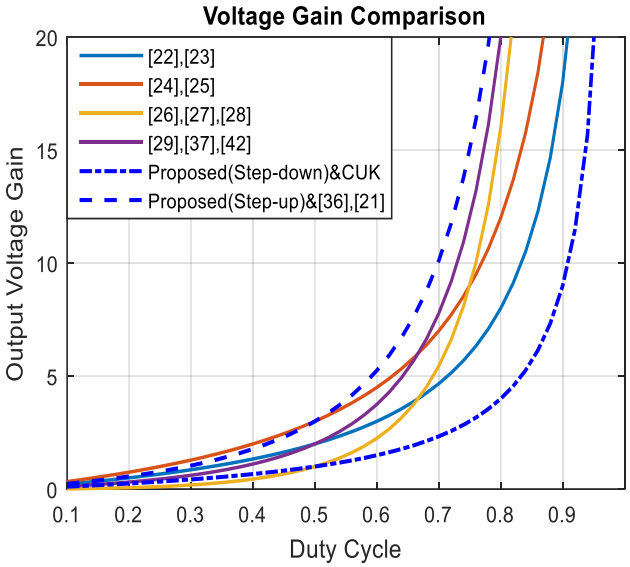


Fig. 13. Voltage gain ratios vs duty cycle comparison

B. Effectiveness Index

In this section, the performance of the provided converter is compared to that of other similar buck-boost converters in order to validate the aforementioned qualities. The complete comparative findings are shown in Table II based on the maximum voltage stress across diodes, common ground characteristics, voltage gain, input/output current ripple, voltage stress on switches, and total number of parts. In addition, an efficiency index (EI) is offered for measuring the ratio between the total number of elements used and the voltage gain value [32, 38]. The EI is calculated as:

$$EI = \frac{\frac{D(2-D)}{(1-D)^2}}{Total\ Number\ of\ Utilized\ Elements} \quad (50)$$

This coefficient accurately represents the best usage of circuit parts and power density in the proposed converter. Fig. 14 depicts the EI vs duty cycle for the recommended converter as well as other comparable converters.

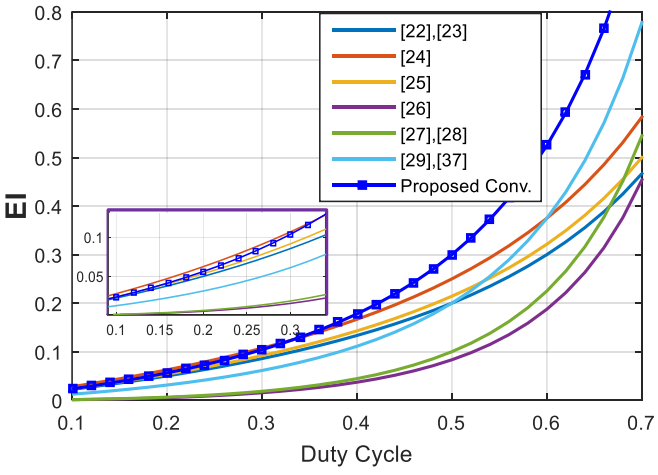


Fig. 14. Effectiveness index.

TABLE I Comparison of Modes (I, II)

Topology	MODES													
	Mode I							Mode II						
	D	**S**	**M_{CCM}**	**C.I/O**	**C.G**	$\sum\frac{V_S}{V_{in}}$	**Norm. SDP_{avg}/P_o**	**D**	**S**	**M_{CCM}**	**C.I/O**	**C.G**	$\sum\frac{V_S}{V_{in}}$	**Norm. SDP_{avg}/P_o**
IN [36]	2	2	$\frac{1-D+D^2}{D(1-D)}$	No/No	Yes	$\frac{1+D}{D(1-D)}$	$\frac{1}{(D-D^2)(1-D+D^2)}$	2	2	$\frac{D(2-D)}{(1-D)^2}$	No/No	Yes	$\frac{2-D}{(1-D)^2}$	$\frac{2}{D(1-D)(2-D)}$
IN [37]	4	2	$\frac{D}{(1-D)^2}$	Yes/No	No	$\frac{2D^2-D+1}{(1-D)^2}$	$\frac{2D^3-D^2+1}{D(1-D)^2}$	3	1	$\left(\frac{D}{1-D}\right)^2$	No/No	No	$\frac{1}{(1-D)^2}$	$\frac{2(D^3-D+1)}{D(1-D)^2}$
Proposed	2	2	$\frac{D(2-D)}{(1-D)^2}$	Yes/Yes	Yes	$\frac{1}{(1-D)^2}$	$\frac{2}{D(1-D)(2-D)}$	1	1	$\frac{D}{1-D}$	Yes/Yes	Yes	$\frac{1}{1-D}$	$\frac{1}{D(2-D)}$

C.I/O= Continuous Input/output, C.G= Common Ground, SDP= Switching Device Power.

TABLE II Comparison of the Buck-Boost Converter and Suggested Converter

Item / Topology	Voltage Gain	Number of Elements*					V_S/V_{in}	V_D/V_{in}	Norm. SDP_{avg}/Po	O.P*	C.I/O*	If M =1
		S	D	C	L	T						
CUK Converter	$\frac{D}{1-D}$	1	1	2	2	6	$\frac{1}{1-D}$	$\frac{1}{1-D}$	----------	(–)	✓/✓	D=0.5
IN [21]	$\frac{D(2-D)}{(1-D)^2}$	1	3	2	2	8	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}\frac{D}{(1-D)^2}$ $\frac{1}{(1-D)^2}$	$\frac{4D^2-4D+2}{D(2-D)(1-D)^2}$	(–)	x/x	D=0.29
IN [22]	$\frac{2D}{1-D}$	1	3	3	3	10	$\frac{1}{1-D}$	$\frac{1}{1-D}\frac{1}{1-D}$	$\frac{2}{D(1-D)}$	(+)	x/✓	D=0.33
IN [23]	$\frac{2D}{1-D}$	1	2	4	3	10	$\frac{1}{1-D}$	$\frac{1}{1-D}\frac{1}{1-D}$	----------	(+)	✓/✓	D=0.33
IN [24]	$\frac{3D}{1-D}$	1	3	5	3	12	$\frac{1}{1-D}$	$\frac{1}{1-D}\frac{2D}{1-D}$ $\frac{1}{1-D}$	$\frac{2}{D(1-D)}$	(–)	x/x	D=0.25
IN [25]	$\frac{3D}{1-D}$	1	3	6	4	14	$\frac{1}{1-D}$	$\frac{1}{1-D}\frac{1}{1-D}\frac{1}{1-D}$	----------	(+)	✓/x	D=0.25
IN [26]	$\left(\frac{D}{1-D}\right)^2$	1	5	3	3	12	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}\frac{D}{(1-D)^2}$ $\frac{1}{(1-D)^2}\frac{1}{1-D}$ $\frac{D}{(1-D)^2}$	$\frac{6D^2-8D+4}{D(1-D)^2}$	(–)	✓/✓	D=0.5
IN [27]	$\left(\frac{D}{1-D}\right)^2$	2	2	3	3	10	$\frac{1}{(1-D)^2}\frac{D}{(1-D)^2}$	$\frac{1}{1-D}\frac{D}{(1-D)^2}$	$\frac{2}{D(1-D)}$	(+)	✓/✓	D=0.5
IN [28]	$\left(\frac{D}{1-D}\right)^2$	2	2	3	3	10	$\frac{1}{1-D}\frac{D}{(1-D)^2}$	$\frac{1}{1-D}\frac{D}{(1-D)^2}$	$\frac{1+D}{D(1-D)}$	(+)	✓/✓	D=0.5
IN [29]	$\frac{D}{(1-D)^2}$	2	2	3	3	10	$\frac{1}{1-D}\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}\frac{D}{(1-D)^2}$	$\frac{1+D}{D(1-D)}$	(–)	✓/✓	D=0.38
IN [36]	$\frac{D(2-D)}{(1-D)^2}$	2	2	2	2	8	$\frac{1}{1-D}\frac{1}{(1-D)^2}$	$\frac{1}{1-D}\frac{1}{(1-D)^2}$	$\frac{2}{D(1-D)(2-D)}$	(–)	x/x	D=0.29
IN [37]	$\frac{D}{(1-D)^2}$	2	4	2	2	10	$\frac{1}{(1-D)^2}$	$1\ \frac{D}{(1-D)^2}$ $\left(\frac{D}{1-D}\right)^2\frac{D}{1-D}$	$\frac{2D^3-D^2+1}{D(1-D)^2}$	(+)	x /x	D=0.38
IN [42]	$\frac{D}{(1-D)^2}$	2	2	2	2	8	$\frac{1}{1-D}\frac{1}{(1-D)^2}$	$\frac{1}{1-D}\frac{1}{(1-D)^2}$	$\frac{1+D}{D(1-D)}$	(–)	✓/x	D=0.38
Proposed	$\frac{D(2-D)}{(1-D)^2}$	2	2	3	3	10	$\frac{1}{1-D}\frac{D}{(1-D)^2}$	$\frac{1}{1-D}\frac{D}{(1-D)^2}$	$\frac{2}{D(1-D)(2-D)}$	(–)	✓/✓	D=0.29

* S=Switch, D= Diode, C= Capacitor, L= Inductor, O.P= Output Polarity, C.I/O= Continuous Input/output, D=Duty cycle.

As shown in the figure, the suggested converter has a greater EI than the converters in [22-29] and [37] over the whole range of feasible duty ratio values. When the duty ratio is smaller than 0.4, the suggested converter and the converters in [24] and [25] have equivalent EI. However, at larger duty ratios, the EI of the suggested buck-boost converter is significantly better than that of current converters. This shows that the suggested converter has a higher power density.

C. Comparison Input Ripple Current

The comparison of input current ripple of the suggested converter with other competitor converters is shown in Fig.15. Fig.15 shows that the input current value of the suggested converter is lower than other buck-boost converters.

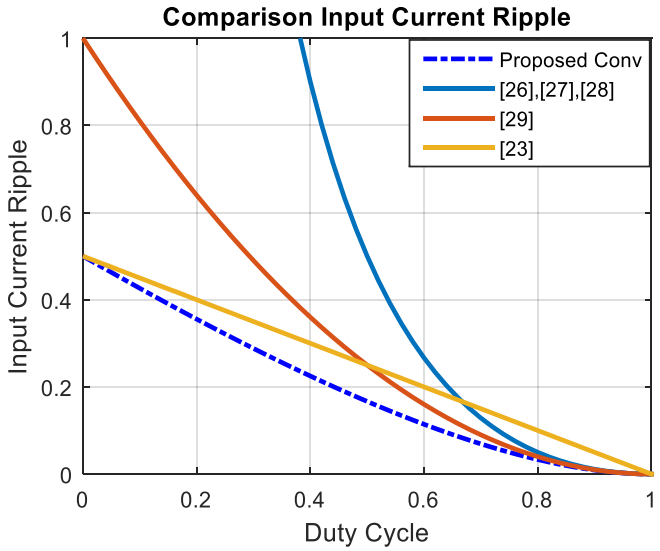


Fig. 15. Comparison the ripple input as a function of duty cycle with other converters.

D. Total Switching Device Power (SDP)

SDP is a useful index for evaluating various switching device aspects such as cooling system requirements, possible expenses, and losses [48, 49]. It is worth noting that the voltage stress and current of the converter's diodes and switches are taken into account when calculating power loss and the overall cost of implementation. The total average switching device power (SDP_{avg}) is expressed as:

$$SDP_{avg} = \sum_{i=1}^{n} V_{S\_i} I_{Savg\_i} \tag{51}$$

In which, I_{Savg_i} and V_{S_i} signify the average current and peak voltage of the ith semiconductor of the power converter during a switching period. Fig. 16 depicts the overall average SDPs for various converters. As can be shown, the suggested converter achieves lower SDP in comparison to previous buck-boost converters by D > 0.5, which directly translates to lower semiconductor cost and power loss. The total average SDP in step-up/down mode is represented as:

$$\begin{cases} Mode\ I: SDP_{avg(Step-up)} = \dfrac{2}{D(1-D)(2-D)} P_o \\ Mode\ II: SDP_{avg(Step-down)} = \dfrac{1}{D(2-D)} P_o \end{cases} \tag{52}$$

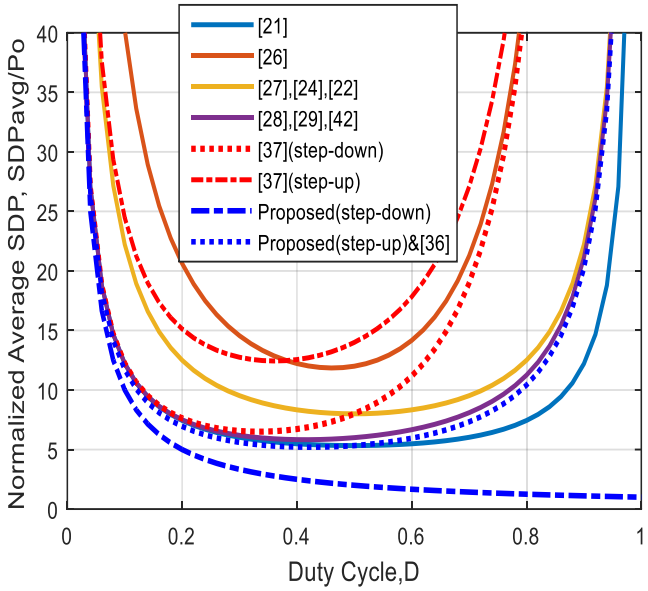


Fig. 16. Comparison of normalized SDPavg.

V. Experimental Verification

To confirm the theoretical claims for both modes of operation, the proposed DC/DC buck-boost converter was experimentally tested and inspected. Table III shows the components used in simulation and experimentation on the suggested converter. The values of these parameters were obtained through the mathematical solution of equations (36) -(38) and (31)- (33). The current ripples of inductors were set at a rate of 30%, whereas the voltage ripples through capacitors C_o, C_2 and C_1 were modified to 0.2, 5 and 5 percent, respectively. The capacitance values of C_o, C_2 and C_1 have been computed utilizing equations (36) -(38). The selection of the inductances of L_3, L_2, and L_1 based on the inductor current ripples as described in equations (31) -(33). In the step-up mode, the desired converter's input voltage level is varied between 15V DC and 60V DC with negative polarity. In the CCM mode, the waveforms of the L_3, L_2, and L_1 inductor currents are examined, together with the converter's input continuous current flow. In addition, with a 15V input voltage source and a duty cycle of 0.553, the mean current of inductors L_3, L_2, and L_1 are 1A, 2.24A, and 4.05A, respectively. The voltages of capacitors C_o, C_2 and C_1 are about -60.05V, -41.54V, and -75.09V, respectively, according to (5) and (6). The power MOSFETs S_2 and S_1, as well as the diodes D_2 and, D_1 were selected based on the components' current stress and voltage. After determining the rating of power MOSFETs and diodes, the mean voltage stress for these four elements is 41.51V, 18.54V, 18.56V, and 14.99V. The average current of inductors L_1, L_2, and L_3 is 0.6A, 0A, and 1A, in step-down mode, when the input voltage is 15V and the duty cycle is 0.375.

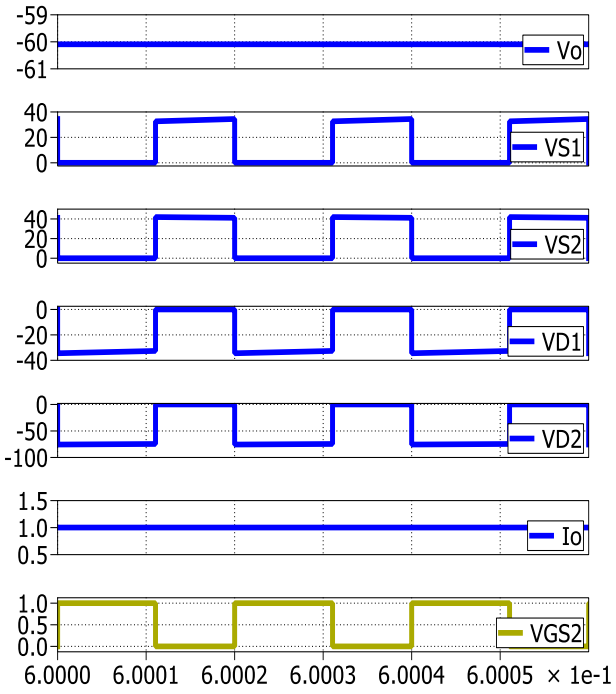
In addition, the voltage stress given to capacitors C_o, C_2 and C_1 is 8.099V, 0V, and -23.99V, respectively. Moreover, the voltage

stresses delivered to power MOSFETs and diodes are 8.99V, 14.99V, 0V, and 8.99V, respectively, based on the analytic formulae.

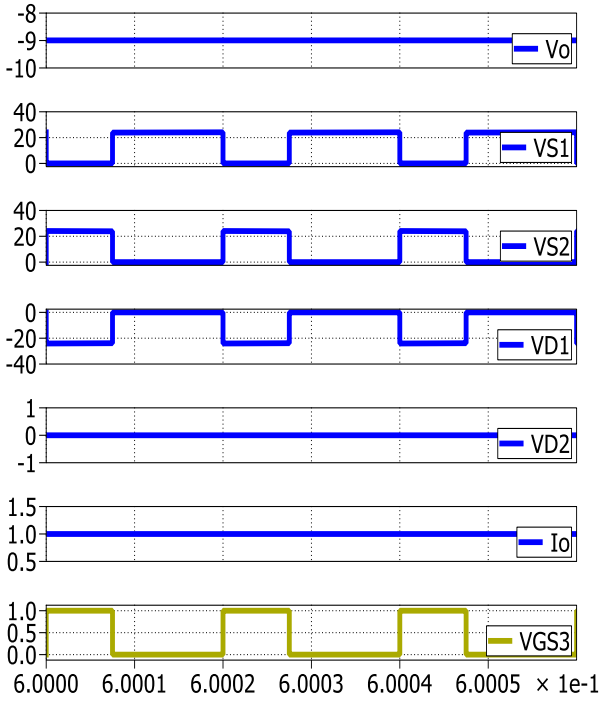
TABLE III Experimental Setup Parameters

Parameters	Mode I	Mode II
	Step-up Mode	Step-down Mode
V_{in}	15V	15V
V_o	**60V**	**9V**
Duty Cycle	0.553	0.375
Output power	60W	9W
fs	50KHz	
L_1, L_2, L_3	138µH, 512µH, 512µH	
R_{L1}, R_{L2} ,R_{L3}	0.064Ω, 0.137Ω, 0.143Ω	
C_1, C_2, Co	33µF, 33µF, 160 µF	
R_{C1}, R_{C2},R_{Co}	0.064Ω, 0.064Ω, 0.022Ω	
S_1,S_2	IRFP4668PBF (R_{DS} = 8mΩ) t_{on} = 41ns, t_{off} = 4ns,$Coss$=810PF	
D_1,D_2	MBR10100 (V_{FD} ~ 0.85V)	

The simulation plots of the investigated converter in the two modes (step-up/down) simulation are shown in Fig.17 while operating in CCM mode through the PLECS software. It represents the current and output voltage, gate-source voltage, diodes voltage, and switch voltage of the MOSFETs. Fig. 17(a) shows the simulation waveforms in PLECS software in the boost mode and Fig. 17(b) shows the simulation waveform in the buck mode.



(a)



(b)

Fig. 17. Simulation waveforms in PLECS. (a) Boost mode; (b) Buck mode.

VI. Hardware Setup and Experimental Evaluation

Here, to verify the aforesaid properties of the suggested converter, an experimental prototype is used. The prototype was run and examined with 9W (buck mode) and 60W (boost mode) output powers. Figs. 18 and 19 show the experimental prototype and the driving circuit. The circuit elements corresponding to the experimental converter are presented in Table III. According to Table III, MOSFETs (IRFP4668PBF). MBR10100 diodes were selected for realizing the circuit.

The photocoupler TLP250 was utilized to drive the power MOSFETS S_1 and S_2. The experimental plots of the experimental prototype are shown in Figs. 20 and 21, which were recorded and measured via a GW INSTEK GDS-2102A oscilloscope and a Pintek PA- 667 1MHz current probes. The plots of the anticipated converter's currents and voltages exhibited in Figs. 20 and 21dual modes indicate a very slight variation between the experimental and PLECS simulation results. Fig. 20(a) depicts the recorded waveforms of the input and output voltage, Fig. 20(b) shows the measured currents of the inductors (L_1, L_2). Fig. 20(c) and Fig. 20(d) illustrate the voltage waveforms of the diodes and power switches in step-down mode, respectively. Fig. 21 shows the same values in step-up mode. Lastly, the test results showed that the proposed converter operation entirely follows the operation principles and characteristics mentioned in the theoretical claims. Fig 22 (a) and (b) show the theoretical and experimental efficiency curves of the proposed converter for varied output power in step-up and step-down modes, respectively.

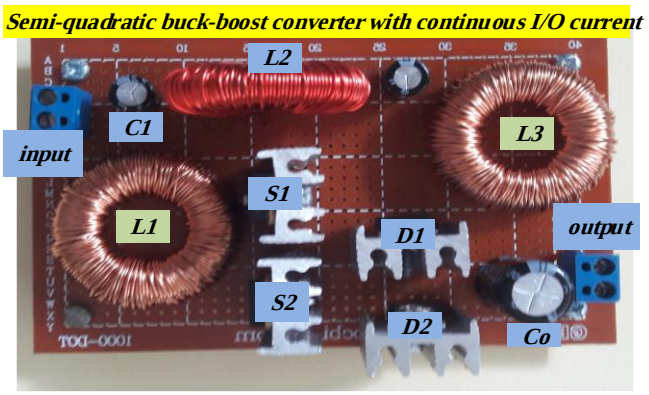


Fig. 18. Experimental hardware prototype.

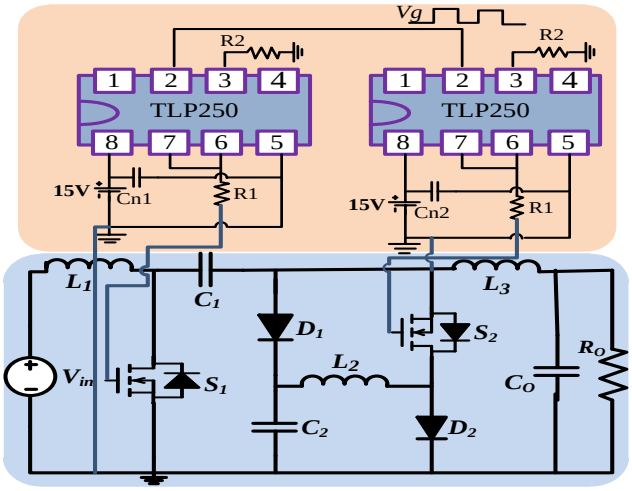
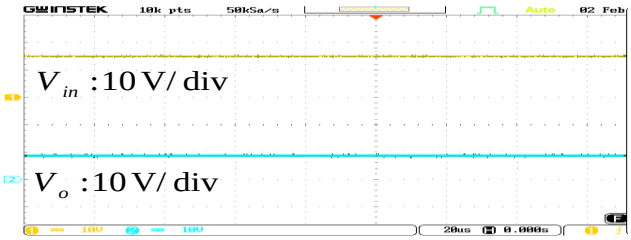
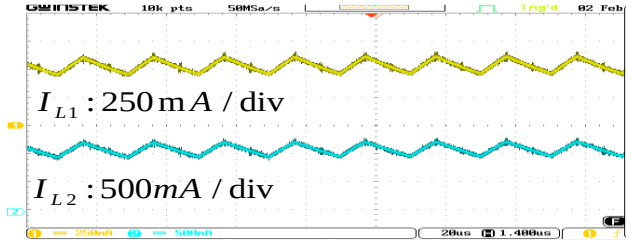


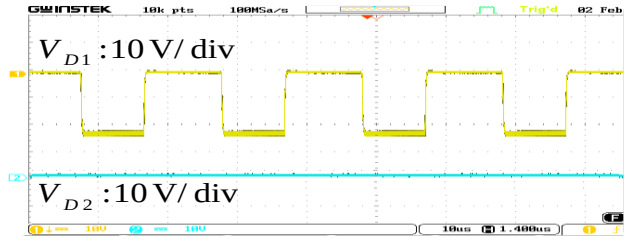
Fig. 19. MOSFET driver circuit



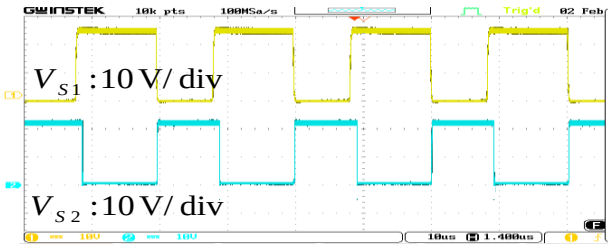
(a)



(b)

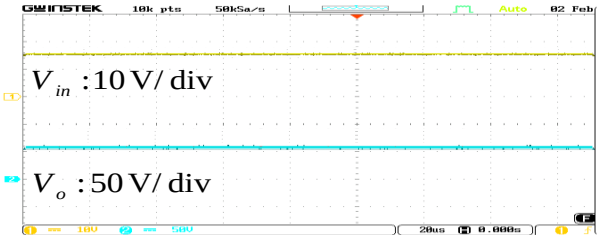


(c)

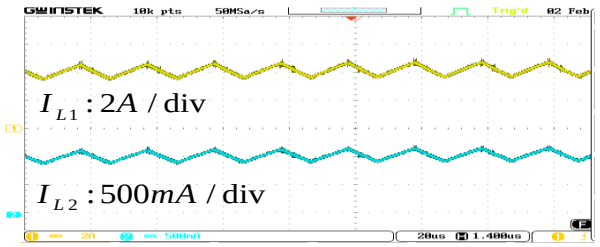


(d)

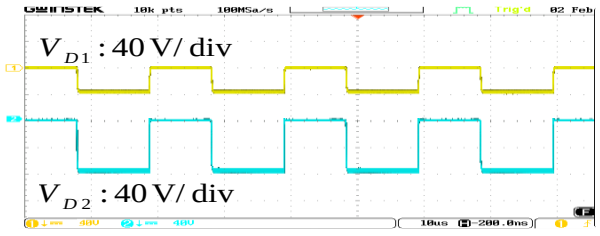
Fig. 20. Waveforms in the step-down mode; (a) V_{in}, V_o; (b) i_{L1}, i_{L2}; (c) V_{D1}, V_{D2}; (d) V_{S1}, V_{S2}.



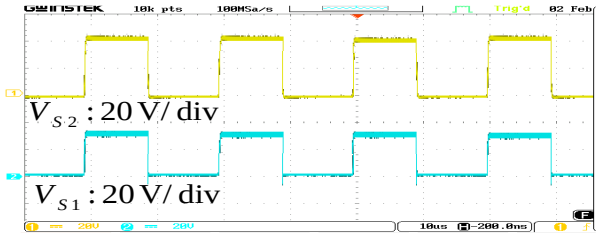
(a)



(b)

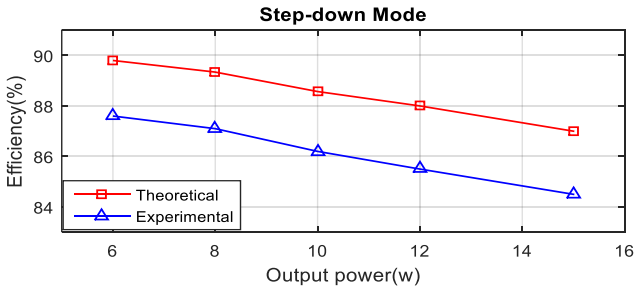


(c)

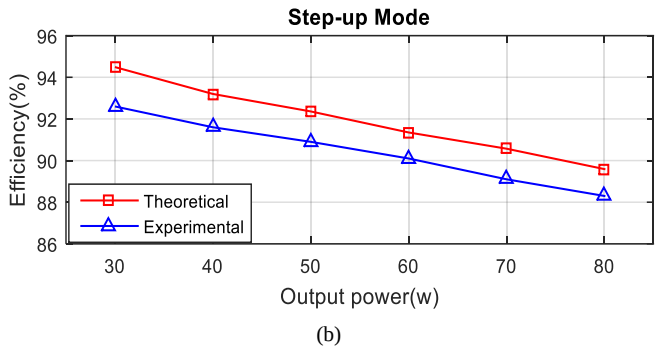


(d)

Fig. 21. Waveforms in the step-up mode; (a) V_{in}, V_o; (b) i_{L1}, i_{L2}; (c) V_{D1}, V_{D2}; (d) V_{S1}, V_{S2}



(a)



(b)

Fig. 22. Efficiency plot of experimental and theoretical result of the suggested converter. (a) Step-down mode (Mode II); (b) Step-up mode (Mode I).

VII. Conclusion

This paper presents a new semi-quadratic DC-DC converter featuring (a) continuous input and output current for reduced ripple and EMI suppression, (b) negative output polarity, (c) wide voltage range operation with minimal duty cycle variation, and (d) dual operating modes offering two distinct buck-boost voltage gain ratios. The working principle was analyzed in both operational modes, with steady-state analysis establishing the relationships between voltage and current. A comprehensive efficiency analysis incorporating component parasitic elements was presented, along with an estimation of power loss. The passive components were designed to meet the requirements for ripple voltage and current. The comparative evaluation demonstrates the converter's superior performance, achieving higher voltage gain, improved efficiency (92.6% in Mode I and 87.6% in Mode II), and lower switching device power (SDP) compared to existing quadratic converters. Experimental validation confirmed the converter's practical performance. With its continuous current characteristics and negative output capability, the proposed topology is particularly suitable for multifunction power supplies, photovoltaic systems, signal generators, audio amplifiers, and data transmission interfaces requiring negative voltage supplies.

REFERENCES

[1] R. Gopi and S. Sreejith, "Converter topologies in photovoltaic applications – A review," *Renew. Sustain. Energy Rev.*, vol. 94, pp. 1-14, 2018, doi: 10.1016/j.rser.2018.05.047.

[2] M. H. Taghvaee, M. A. M. Radzi, S. M. Moosavain, H. Hizam, and M. H. Marhaban, "A current and future study on non-isolated DC–DC converters for photovoltaic applications," *Renew. Sustain. Energy Rev.*, vol. 17, pp. 216-227, 2013, doi: 10.1016/j.asej.2021.06.027

[3] F. Blaabjerg, R. Teodorescu, Z. Chen, and M. Liserre, "Power converters and control of renewable energy systems," in *Proc. 6th Int. Conf. Power Electron*, pp. 1-20, Oct 18, 2004.

[4] F. Blaabjerg, C. Zhe, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, pp. 1184-1194, 2004, doi: 10.1109/TPEL.2004.833453.

[5] K. Nathan, S. Ghosh, Y. Siwakoti and T. Long, "A new dc–dc converter for photovoltaic systems: coupled-inductors combined cuk-sepic converter, " *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 191-201, Mar 2019, doi: 10.1109/TEC.2018.2876454

[6] A. Torkan and M. Ehsani, "A novel nonisolated z-source dc–dc converter for photovoltaic applications, " *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 4574-4583, Sept.-Oct. 2018, doi:10.1109/TIA.2018.2833821

[7] K. V. G. Raghavendra, et al. "A comprehensive review of DC–DC converter topologies and modulation strategies with recent advances in solar photovoltaic systems, " *J. Electron.*; vol. 9, no. 1, Dec 26, 2019, doi:10.3390/electronics9010031.

[8] L. J. Jeremy, C.A. Ooi, J. Teh, " Non-isolated conventional DC-DC converter comparison for a photovoltaic system: a review," *J. Renew. Sustain. Energy*; vol. 12, no. 1, 2020, doi:10.1063/1.5095811.

[9] R. W. Erickson and D. Maksimovic, in *Fundamentals of power electronics*, 2nd ed. Boston: Kluwer Academic Publishers, 2001.

[10] F. Mumtaz, N. Z. Yahaya, S. T. Meraj, B. Singh, R. Kannan, and O. Ibrahim, "Review on non-isolated DC-DC converters and their control techniques for renewable energy applications," *Ain Shams Eng. J.*, 2021, doi: 10.1109/TIE.2016.2608321.

[11] M. Adly and K. Strunz, "Irradiance-adaptive pv module integrated converter for high efficiency and power quality in standalone and dc microgrid applications," IEEE Trans. Ind. Electron., vol. 65, pp. 436-446, 2018, doi: 10.1109/TIE.2017.2723860.

[12] S. Chen, T. Liang and K. Hu, “Design, analysis, and implementation of solar power optimizer for dc distribution system,” in *IEEE Trans. Power Electron.*, vol. 28, no. 4, pp. 1764-1772, April 2013, **doi:** 10.1109/TPEL.2012.2213270.

[13] “SolarEdge Fixed String Voltage, Concept of Operation,” [Online]. Available: https://www.solaredge.com.

[14] J. D. Navamani, K. Vijayakumar, R. Jegatheesan, " Non-isolated high gain DC/DC converter by quadratic boost converter and voltage multiplier cell, " *Ain Shams Eng. J.*; pp.1397–406, 2018.

[15] J. D. Navamani, A. Lavanya, D. Almakhles, and M. J. Sathik, “A review on segregation of various high gain converter configurations for distributed energy sources,” *Alexandria Eng. J.*, vol. 61, no. 1, pp. 675-700, Jan 2022, doi: 10.1109/JESTPE.2022.2985844.

[16] K. I. Hwu and T. J. Peng, "A novel buck–boost converter combining ky and buck converters," *IEEE Trans. Power Electron.*, vol. 27, pp. 2236-2241, 2012, doi**:** 10.1109/TPEL.2011.2182208.

[17] H. Ardi and A. Ajami, "Study on a high voltage gain sepic-based dc–dc converter with continuous input current for sustainable energy applications," *IEEE Trans. Power Electron.*, vol. 33, pp. 10403-10409, 2018, doi: 10.1109/TPEL.2018.2811123.

[18] S. Miao, F. Wang, and X. Ma, "A new transformerless buck–boost converter with positive output voltage," *IEEE Trans. Ind. Electron.*, vol. 63, pp. 2965-2975, 2016, doi: 10.1109/TIE.2016.2518118

[19] M. R. Banaei, H. Ardi, and A. Farakhor, "Analysis and implementation of a new single-switch buck-boost dc/dc converter," *IET Power Electron.*, vol. 7, pp. 1906-1914, 2014, doi: 10.1049/iet-pel.2013.0762.

[20] J. C. Rosas-Caro, J. E. Valdez-Resendiz, J. C. Mayo-Maldonado, A. Alejo-Reyes, and A. Valderrabano-Gonzalez, "Quadratic buck–boost converter with positive output voltage and minimum ripple point design," *IET Power Electron.*, vol. 11, pp. 1306-1313, 2018, doi:10.1049/iet-pel.2017.0090.

[21] S. A. Gorji, A. Mostaan, H. T. My, and M. Ektesabi, "Non-isolated buck–boost dc–dc converter with quadratic voltage gain

ratio," *IET Power Electron.,* vol. 12, pp. 1425-1433, 2019, doi:10.1049/iet-pel.2018.5703.

[22] M. R. Banaei, and H. A. F. Bonab, "A high efficiency non-isolated buck-boost converter based on zeta converter, " *IEEE Trans. Ind. Electron.*, pp. 1-1, 2019, doi: 10.1109/TIE.2019.2902785.

[23] S. H. Hosseini, R. Ghazi, and S. K. Movahhed, "A novel high gain single-switch dc-dc buck-boost converter with continuous input and output power," at the *24th IEEE Elect. Power Distribution Conf. (EPDC),* Khorramabad, Iran, pp. 10-15, 2019, doi: 10.1109/EPDC.2019.8903599.

[24] M. R. Banaei and H. A. F. Bonab, "A novel structure for single-switch nonisolated transformerless buck-boost dc-dc converter," *IEEE Trans. Ind. Electron.*, vol. 64, no. 1, pp. 198-205, Jan. 2017, doi: 10.1109/TIE.2016.2608321.

[25] M. R. Banaei, and S. G. Sani, "Analysis and implementation of a new sepic-based single-switch buck-boost dc-dc converter with continuous input current" *IEEE Trans. on Power Electronics*, vol. 33, no. 12, pp. 10317–10325, 2018, doi: 10.1109/TPEL.2018.2799876.

[26] N. Zhang, G. Zhang, K. W. See, and B. Zhang, "A single-switch quadratic buck–boost converter with continuous input port current and continuous output port current," *IEEE Trans. Power Electron.*, vol. 33, pp. 4157-4166, 2018, doi: 10.1109/TPEL.2017.2717462.

[27] A. Sarikhani, B. Allahverdinejad, M. Hamzeh, and E. Afjei, "A continuous input and output current quadratic buck-boost converter with positive output voltage for photovoltaic applications," *J. Sol. Energy*, vol. 188, pp. 19-27, 2019, doi:10.1016/j.solener.2019.05.025.

[28] M. Veerachary, M.R. Khuntia, "Design and analysis of two-switch-based enhanced gain buck–boost converters". *IEEE Trans. Ind. Electron*., vol. 69, no. 4, pp. 3577–3587, 2022, doi:10.1109/TIE.2021.3071696.

[29] M. Okati, M. Eslami, M. J. Shahbazzadeh, H. Shareef, "A new transformerless quadratic buck–boost converter with high voltage gain ratio and continuous input/output current port,". *IET Power Electron.,* vol. 15, no. 13, pp. 1280-1294, 2022, doi: 10.1049/pel2.12304.

[30] P. K. Maroti, S. Padmanaban, J. B. Holm-Nielse, M. S. Bhaskar, M. Meraj, A. Iqbal, "A new structure of high voltage gain SEPIC converter for renewable energy application, ". *IEEE Access*, vol. 7, pp. 89857–89868, 2019, doi: 10.1109/ACCESS.2019.2925564.

[31] J. C. Mayo-Maldonado, J. E. Valdez-Resendiz, P. M. Garcia-Vite, J. C. Rosas-Caro, M. R. Rivera-Espinosa and A. Valderrabano-Gonzalez, "Quadratic buck–boost converter with zero output voltage ripple at a selectable operating point," *IEEE Trans. Ind. Appl.*, vol. 55, no. 3, pp. 2813-2822, May-June 2019, doi: 10.1109/ACCESS.2019.2925564.

[32] K. Yari, S. H. Shahalami and H. Mojallali, "A novel nonisolated buck–boost converter with continuous input current and semiquadratic voltage gain," in *IEEE J. Emerg. and Sel. Topics in Power Electron.*, vol. 9, no. 5, pp. 6124-6138, Oct. 2021, doi: 10.1109/JESTPE.2021.3069788.

[33] M. Okati, M. Eslami & M. J. Shahbazzadeh, "A non-isolated dc-dc converter with dual working modes and positive output voltage", *Electric Power Compon. and Syst.*, vol.49, pp. 1143-1157, 2022, doi: 10.1080/15325008.2022.2049662.

[34] A. Mahmood et al., "A non-inverting high gain dc-dc converter with continuous input current," in *IEEE Access*, vol. 9, pp. 54710-54721, 2021, doi: 10.1109/ACCESS.2021.3070554.

[35] A. Sarikhani, B. Allahverdinejad, M. Hamzeh, "A nonisolated buck–boost DC–DC converter with continuous input current for photovoltaic applications," in *IEEE J. Emerg. Sel. Top. Power Electron*, vol. 9, pp.804–811, 2021, doi: 10.1109/JESTPE.2020.2985844.

[36] J. Li and J. Liu, "A negative-output high quadratic conversion ratio dc-dc converter with dual working modes," *IEEE Trans. Power Electron*., vol. 34, no. 6, pp. 5563-5578, June 2019, doi: 10.1109/TPEL.2018.2870421.

[37] M. A. Abbaszadeh, M. Monfared, and H. Heydari-doostabad, "High buck in buck and high boost in boost dual-mode inverter (Hb^2DMI)," *IEEE Trans. Ind. Electron.*, vol. 68, pp. 4838-4847, 2021, doi: 10.1109/TIE.2020.2988240.

[38] S. Hasanpour, A. Baghramian and H. Mojallali, "analysis and modeling of a new coupled-inductor buck–boost dc–dc converter for renewable energy applications," in *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8088-8101, Aug. 2020, doi: 10.1109/TPEL.2019.2962325.

[39] H. Gholizadeh, S. A. Gorji and D. Sera, "A Quadratic Buck-Boost Converter with Continuous Input and Output Currents," in *IEEE Access*, vol. 11, pp. 22376-22393, 2023, doi: 10.1109/ ACCESS.2023.2981331.

[40] S. A. Gorji, "Reconfigurable Quadratic Converters for Electrolyzers Utilized in DC Microgrids," in *IEEE Access*, vol. 10, pp. 109677-109687, 2022, doi: 10.1109/ACCESS.2022.3214581

[41] S. Miao, N. Lyu, X. Jiang, W. Liu and Y. Jin, "A New Fifth-Order Boost Converter with Dual Operating Modes and Wider Conversion Ratios for Renewable Energy Applications," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 12, pp. 4914-4918, Dec. 2022, doi: 10.1109/TCSII.2022.3192641.

[42] SVK. Naresh, S. Peddapati. "Complementary switching enabled cascaded boost-buck-boost (BS-BB) and buck-boost-buck (BB-BU) converters". *Int J Circ Theor Appl*, vol. 49, no. 9, pp. 2736–2753. 2021, doi: 10.1002/cta.3034.

[43] S. Toofan, B. Fathipour, and E. Babaei, "A Single Switch Transformer-Less DC-DC Converter with Continuous Input Current for Photovoltaic Applications,". *International Journal of Industrial Electronics Control and Optimization*, vol. 7, no. 4, pp. 281-290, 2024, doi:10.22111/ieco.2024.48295.1548.

[44] H. Gholizadeh, and S. Hasanpour, "A New Quadratic CUK-Based Step-Up DC/DC Converter Without Right Hand Plane Zero", *International Journal of Industrial Electronics Control and Optimization*, vol. 8, no. 1, pp. 25-35, 2025, doi.:10.22111/ieco.2024.48683.1565.

[45] M. Elmi, M.R. Banaei, and H. Afsharirad, "Study on a Non-Isolated High Step-Up SEPIC-Based DC-DC Converter with Continuous Input Current for Photovoltaic Applications", *International Journal of Industrial Electronics Control and* Optimization, vol. 8, no. 1, pp. 95-104, 2025, doi: 10.22111/ieco.2024.48587.1558.

[46] K. Yari, S. Hasanpour. "A Minimum Phase DC-DC Converter with Continuous Input Current and High Voltage Gain", *International Journal of Industrial Electronics Control and Optimization*, vol. 7, no. 4, pp. 301-312, 2024, doi:10.22111/ieco.2024.48842.1572.

[47] R. D. Middlebrook, "Small-signal modeling of pulse-width modulated switched-mode power converters," *Proc. of the IEEE*, vol. 76, pp. 343-354, 1988, doi: 10.1109/5.4421.

[48] Y. Zhang, J. Liu, X. Ma, J. Feng, "Comparison of conventional DC-DC converter and a family of diode-assisted DC-DC converter in renewable energy applications, *"Journal of Power Electron*. vol. 14, pp. 203–216, 2014, doi:10.6113/JPE.2014.14.2.203.

[49] M. Shen, A. Joseph, J. Wang, F. Z. Peng, and D. J. Adams, "Comparison of traditional inverters and z -source inverter for fuel cell vehicles," *IEEE Trans. Power Electron.*, vol. 22, pp. 1453-1463, 2007, doi: 10.1109/TPEL.2007.900505.

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