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Novel Low-Power OTA using New Block to Eliminate Common-Mode Signal

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ABSTRACT

In this paper, a trans-conductance amplifier based on Common Mode Rejection Ratio (CMRR) enhancement block is presented. The proposed block is capable of eliminating common mode signals at input stage. This feature improves the gain and CMRR of the amplifier substantially. The Cascode structure is also eliminated in proposed architecture, which resulted in favorably reduced power consumption due to low supply voltage requirements. The presented OTA is simulated in 180nm CMOS technology at Cadence Spectre environment with 1.5 v supply voltage proving it appropriate for low-voltage applications. The bias current of the proposed circuit is very low value of 3.9 µA. Gain and phase margin for this block are achieved to be 83.96 dB and 61.68 degree, respectively. These results achieved while the circuit drive a 5pF load at its output. The power consumption of the proposed amplifier is interestingly very low value of 5.9 µW which makes the block suitable for low-power applications.

I. Introduction

Operational amplifiers are one of the most important and widely used blocks in many analog circuits such as data converters, switched capacitor circuits and filters and medical circuits [1-3]. In switched-capacitor circuits, CMOS OTAs are widely used to transfer the charge between the capacitors with the targeted accuracy [4, 5]. Due to the rapid development of CMOS technology and the rapid growth of portable electronic devices, the demand for power-efficient integrated circuits has been increased [6]. On the other hand, down-scaling the device sizes along with smaller power supply requirements has forced the designers to make use of low-voltage, low-power techniques [7]. Meanwhile, decreasing the power supply voltage can reduce the voltage dynamic range and impose other restrictions such as current trasfer inefficiency on the circuit [8, 9]. Thus performance enhancement of advanced recycling folded cascode is always on demand [10].

Single stage amplifiers, such as Folded Cascode (FC) and telescopic amplifiers are more appropriate for low power applications compared with the two stage amplifiers due to their lower power consumption. Folded Cascode amplifiers have higher gain-bandwidth and higher output voltage swing, in comparison with their telescopic counterparts, and have therefore been widely used in recent years [11]. Meanwhile, easily connecting the output to input in folded cascode amplifier to build a buffer is another advantage of these amplifiers [12]. In Folded Cascode amplifiers, bias current sources have no role at improving the amplifier performance, so recycling bias current has been introduced as a technique to improve the gain and power consumption of amplifiers by handling the bias current source values [13].

RFC structure originally proposed at [14], in which the RFC scheme is thoroughly scrutinized and its benefits over the conventional FC structure approved by mathematical calculations and CAD tool simulations.

To improve the performance of Folded Cascode amplifier, the RFC structure is proposed in [15]. The relative isolation of the AC current path from the DC one, has lead to a significant increase in the gain and the slew rate of the amplifier compared with the conventional Folded Cascode amplifier, imposing no increase in surface area and power

consumption of the structure. The fact that the AC and DC paths are not full isolation from each other in this structure, leads to the amplifier trans-conductance being limited, which this problem has been fixed by the use of IRFC and the full isolation of AC and DC current paths [16].

In this paper, a new amplifier based on RFC structure is represented which includes the new CMRR enhancement block at its input stage. This block is capable to strictly remove the common mode current. The proposed amplifier, possesses the requirements for optimum performance, including very lower power consumption, bias current and supply voltage, higher gain and the reliably sufficient phase margin. Using compensation resistor, certain phase margin for the circuit is obtained [17].

This article includes the following sections: in section II the proposed amplifier is analyzed and discussed. Section III contains various parameters and simulation results obtained for the circuit. And finally, the article ends with conclusions in Section IV.

II. Principle of Operation

As shown in Fig. 1, the proposed amplifier has two stages, namely, the input and output stages. The CMRR enhancement block which is incorporated at input stage of the proposed amplifier, makes it possible to eliminate the common mode currents at input stage. This leads to a significant improvement of the amplifier's CMRR. In the conventional RFC structures, the Cascode structures are used in order to increase the accuracy of the signal transmission and thereby improving at CMRR. However, due to the Cascode structures utilized, this circuit requires a relatively high supply voltage, which will increase the overall power consumption. But, in the proposed circuit due to the fundamental role of the CMRR strengthening blocks in eliminating the common mode signals, simple current mirrors are efficiently utilized, interestingly reducing the minimum required supply voltage. This block is shown in Fig. 1 with dashed line. Also, in proposed amplifier the Cascode stage DC bias voltage that is required for the performance of transistors of the amplifiers is eliminated. A pair of PMOS transistors is used at the input of the amplifier because of lower common mode voltage input and flicker noise and higher non-dominant pole compared to the NMOS pair. Likewise, in the output stage, a low-voltage Cascode current mirror is placed that creates the bias voltage for the transistors of Cascode utilizing the input current.

The CMRR enhancement performance of the block at eliminating the common mode signal will be discussed below, by equivalent small-signal analysis of the proposed amplifier. In Fig. 2, half equivalent small-signal circuit of the amplifier is shown. Analyzing this circuit, it appears that due to a large equivalent resistance at node C_1, the current delivered to the output stage will be accompanied by a trivial error.

In Fig. 2, resistors and voltages of the M_n transistor connected to CMRR enhancement block, are called R_n and V_n, respectively and is defined by small signal analysis as follows:

$$R_{14} = \frac{h.rds_0(1+\mu_{2a}) + rds_{2a} + rds_{14}}{1+\mu_{14}} \quad (1)$$

$$R_{15} = \frac{h.rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}{1+\mu_{15}} \quad (2)$$

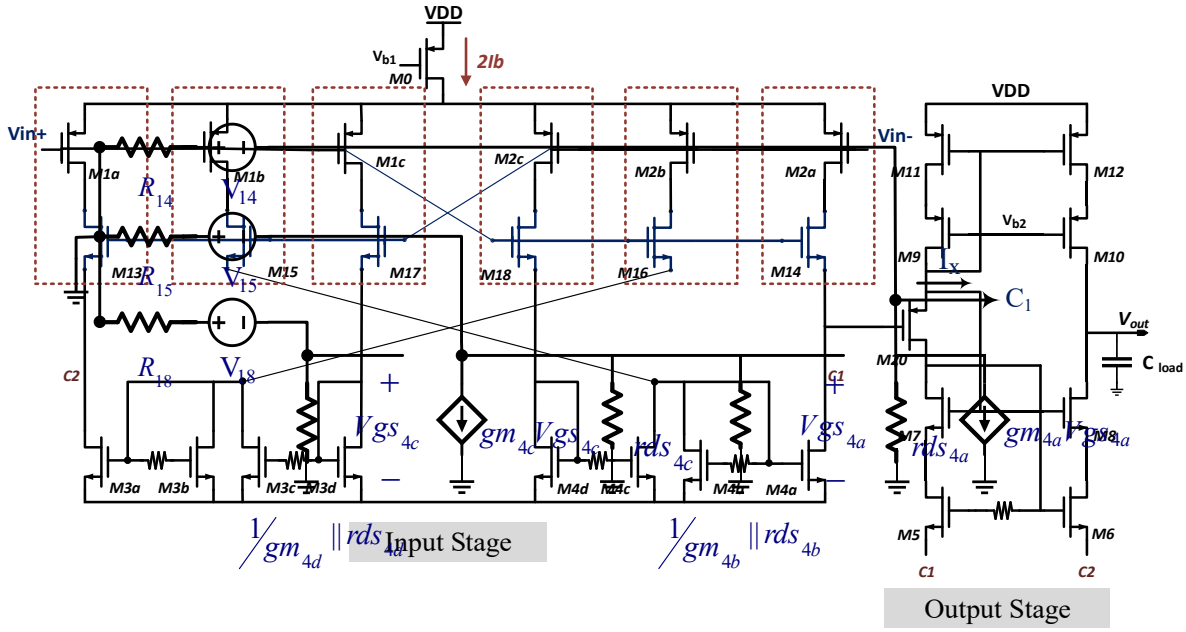


Fig. 2. The equivalent half circuit for input stage of OTA

Fig. 1. The proposed OTA based on CMRR enhancement block

$$R_{18} = \frac{h.rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}}{1+\mu_{18}} \quad (3)$$

$$V_{14} = \frac{Vin_1\mu_{2a} - Vin_2\mu_{14}}{1+\mu_{14}} \quad (4)$$

$$V_{15} = \frac{Vin_2\mu_{1b} - Vin_1\mu_{15}}{1+\mu_{15}} \quad (5)$$

$$V_{18} = \frac{Vin_1\mu_{2c} - Vin_2\mu_{18}}{1+\mu_{18}} \quad (6)$$

$$\begin{matrix} Vin_1 = Vin_- \\ Vin_2 = Vin_+ \end{matrix} \quad (7)$$

Parameter, h, is zero for differentional mode and is one for common mode. gm_i is ith mosfet transconductance, rds_i is ith mosfet output intrinsic impedance and $\mu_i = gm_i \times rds_i$.

Considering the Fig. 1, it can be seen that currents are passed from the input stage through nodes C_1 and C_2 to the output one.
where

The half equivalent circuit includes node C_1, whoes current is named I_x. According to Fig. 2, I_x can written as:

$$\begin{matrix} I_x \\ = gm_{4a}Vgs_{4a} \\ + \frac{Vin_1\mu_{2a} - Vin_2\mu_{14}}{\boldsymbol{h}.rds_0(1+\mu_{2a}) + rds_{2a} + rds_{14}} \end{matrix} \quad (8)$$

Where V_{gs4a}, is gate-source voltage of transistor M_{4a} and can be calculated by small signal analysis of the Figure 2 as follows:

$$\begin{matrix} Vgs_{4a} = [\frac{1}{gm_{4b}} || rds_{4b} || rds_{4c} || R_{15}] \times \\ (gm_{4c}Vgs_{4c} \\ + \frac{Vin_2\mu_{1b} - Vin_1\mu_{15}}{h.rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}) \end{matrix} \quad (9)$$

$$\begin{matrix} Vgs_{4c} = [\frac{1}{gm_{4d}} || rds_{4d} || R_{18}] \times \\ (\frac{Vin_1\mu_{2c} - Vin_2\mu_{18}}{h.rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}}) \end{matrix} \quad (10)$$

By calculating the value of the parameter gate-source voltage of the transistor and putting it in Eq. (8), I_x is obtained as:

$$I_x = Vin_1(F) - Vin_2(G) \quad (11)$$

where F and G, are coefficients of V_{in1} and V_{in2}, respectively and can be calculated as follows:

$$\begin{matrix} F = [\frac{gm_{4a}}{gm_{4b}}(\frac{gm_{4c}\mu_{2c}}{gm_{4d}\,\mathrm{h.rds}_0(1+\mu_{2c}) + (rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}} \\ - \frac{\mu_{15}}{rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}) + \frac{\mu_{2a}}{rds_0(1+\mu_{2a}) + rds_{14} + rds_{2a}}] \end{matrix} \quad (12)$$

$$\begin{matrix} G = [\frac{gm_{4a}}{gm_{4b}}(\frac{gm_{4c}\mu_{18}}{gm_{4d}\,\mathrm{h}.rds_0(1+\mu_{2c}) + rds_{2c} + rds_{18}} \\ - \frac{\mu_{1b}}{rds_0(1+\mu_{1b}) + rds_{1b} + rds_{15}}) \\ + \frac{\mu_{14}}{rds_0(1+\mu_{2a}) + rds_{14} + rds_{2a}}] \end{matrix} \quad (13)$$

It can be observed that for equal values of the F and G, the voltages V_{in1} and V_{in2} in common mode have same sign and value of I_x will be zero, and as a consequence the CMRR approaches to infinite. Due to the opposite sign of the differential mode input voltages, the input stage current will be transferred to the output stage with doubled amplification.

For the coefficients F and G in node C_1 being equal, Eq. (14) must apply.

$$\begin{cases} \mu_{18} = \mu_{2c} \\ \mu_{15} = \mu_{1b} \\ \mu_{14} = \mu_{2a} \end{cases} \quad (14)$$

If we name the current transferred from node C_2 to the output stage, I_y, then for another half equivalent circuit similar to the one exhibited above its value can be calculated. Detailed equations related to I_y is neglected to avoid paper enlarment.

$$I_y = Vin_2(N) - Vin_1(M) \quad (15)$$

where M and N, are coefficients of V_{in1} and V_{in2}, respectively and can be calculated as follows:

$$\begin{matrix} M = [\frac{gm_{3a}}{gm_{3b}}(\frac{gm_{3c}\mu_{17}}{gm_{3d}\,\mathrm{h}.\mathrm{rds}_0(1+\mu_{1c}) + (rds_{1c} + rds_{17})} \\ - \frac{\mu_{2b}}{rds_0(1+\mu_{2b}) + rds_{2b} + rds_{16}}) \\ + \frac{\mu_{13}}{rds_0(1+\mu_{1a}) + rds_{1a} + rds_{13}}] \end{matrix} \quad (16)$$

$$\begin{matrix} N = [\frac{gm_{3a}}{gm_{3b}}(\frac{gm_{3c}\mu_{1c}}{gm_{3d}\,\mathrm{h}.\mathrm{rds}_0(1+\mu_{1c}) + (rds_{1c} + rds_{17})} \\ - \frac{\mu_{16}}{rds_0(1+\mu_{2b}) + rds_{2b} + rds_{16}}) \\ + \frac{\mu_{1a}}{rds_0(1+\mu_{1a}) + rds_{1a} + rds_{13}}] \end{matrix} \quad (17)$$

For the coefficients M and N in node C_2 being equal, Eq. (18) must apply.

$$\begin{cases} \mu_{17} = \mu_{1c} \\ \mu_{16} = \mu_{2b} \\ \mu_{13} = \mu_{1a} \end{cases} \quad (18)$$

Further scrutinizing the equations in differential and common mode CMRR can be achieved as follows:

$$CMRR = \frac{A_d}{A_c} = \frac{A(F+G) - B(M+N)}{A(F-G) - B(M-N)} \quad (19)$$

where A and B are defined as follows:

$$A = R_z(K_2\, gm_8 + K_1 R_K gm_6) + K_2 gm_{12}(R_K + rds_8) \quad (20)$$

$$B = R_K . R_z$$

$$R_z = \frac{rds_{12} + rds_{10}}{1 + \mu_{10}} \quad (21)$$

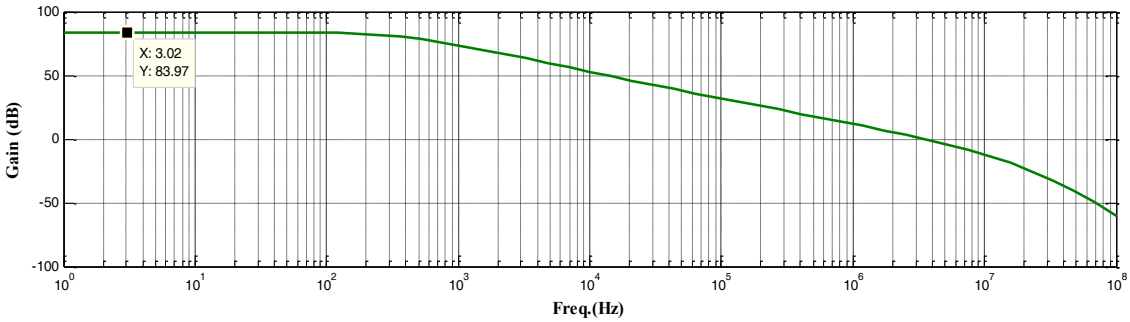
$$R_K = (R_{13} || rds_{3a} || rds_6)(1 + \mu_8) \quad (22)$$

$$K_1 = \frac{[\frac{\mu_7}{gm_5} - \frac{\mu_{20}}{rds_{20} + R(1+\mu_{20})}]}{1 - gm_5[\frac{\mu_7}{gm_5} - \frac{\mu_{20}}{rds_{20} + R(1+\mu_{20})}]} \quad (23)$$

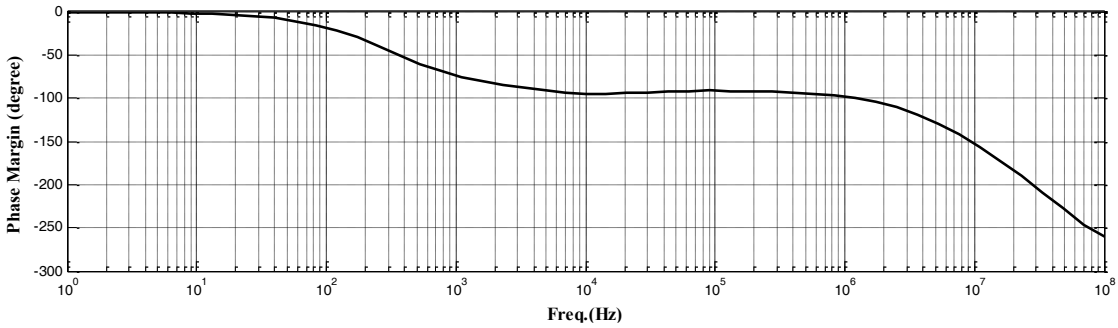
$$K_2 = \frac{\frac{1}{gm_5}}{1 - \mu_7 + \frac{\mu_{20}}{gm_5(rds_{20} + R(1+\mu_{20})}} \quad (24)$$

Theoretically, for F=G and M=N upon establishment of the Eq. (14) and Eq. (18), the required circumstances of the proposed block placed in the input stage of amplifier are fulfilled and the role of this block in eliminating the common mode signal and increasing the CMRR is achieved. In this circumstance, the denumerator becomes zero and CMRR approaches infinite values.

One way to relax the phase margin of the amplifier, is to put a compensation resistance between NMOS current mirror transistors to separate their parasitic capacitances. By placing this resistor, as shown in Fig. 3, the first order transfer function current mirror becomes a second order transfer function current mirror. The transfer function of the current mirror shown in Fig. 3, can be written as follows to obtain its zero/poles



(a)



(b)

Fig. 4. (a) DC gain and (b) phase margin's curve of the proposed OTA

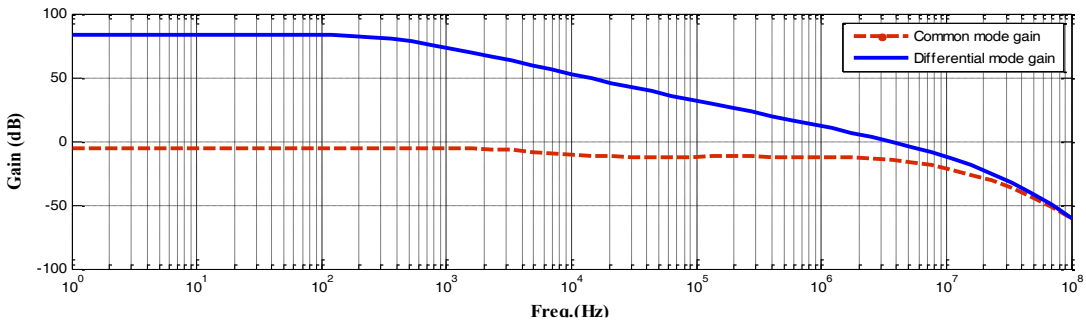


Fig. 5. Differential and common mode gain

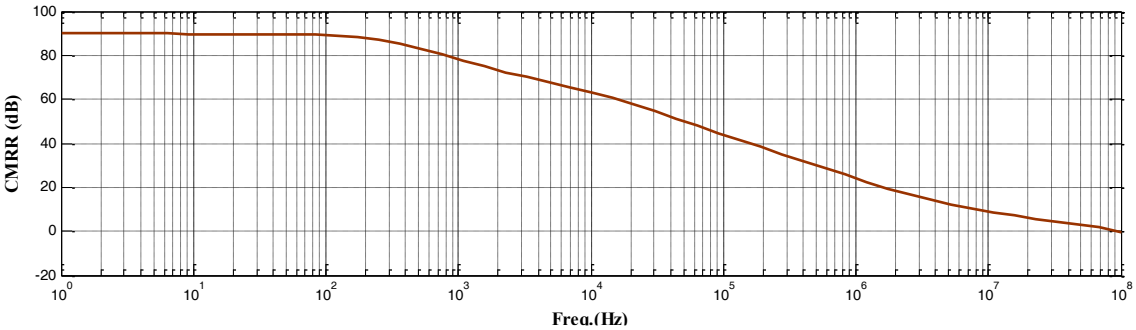


Fig. 6. CMRR curve of the proposed OTA

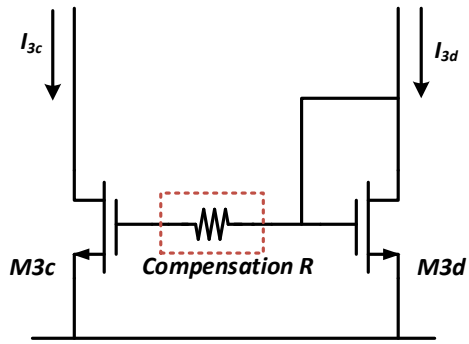


Fig. 3. Current mirror used in the proposed amplifier with compensation resistance

$$H(s) = \left(\frac{gm_{3c}}{gm_{3d}}\right)\frac{sRCgs_{3d}+1}{s^2\frac{RCgs_{3d}Cgs_{3c}}{gm_{3d}}+s\frac{Cgs_{3d}+Cgs_{3c}}{gm_{3d}}+1} \quad (25)$$

The current mirror transfer function zero/poles are obtained as below:

$$z = -\frac{1}{RCgs_{3d}} \quad (26)$$

$$p_{1,2} = \frac{Cgs_{3d}+Cgs_{3c}}{2RCgs_{3d}Cgs_{3c}}\left[-1 \pm \sqrt{1-\frac{4RCgs_{3c}Cgs_{3d}gm_{3d}}{(Cgs_{3c}+Cgs_{3d})^2}}\right] \quad (27)$$

Considering these equations, one can see that the first order transfer function current mirror is modified to yield a second order transfer function current mirror including a zero and two poles. The zero incorporated to the transfer function of the proposed amplifier, makes the system to operate faster. For each specific application and system the design must be customized to achieve the optimum performance. Modifying the value of aforementioned compensation resistance can reshape zero-pole pattern of the transfer function to yield optimum performance for any custom design and/or application.

III. Simulation Results

To prove the performance of the proposed amplifier, this circuit is simulated at Cadence software with 180nm CMOS technology while driving a 5pF load at its output. The Cascode structure which is commonly used at conventional RFC amplifiers has been removed because it requires a high supply voltage. Hence, the power supply voltage and accordingly the power consumption have been relatively diminished. The bias current of the proposed circuit is obtained 3.9μA for supply voltage of 1.5v. The power consumption is achieved to be 5.9μw which is suitable for low voltage and low power applications.

The DC gain and phase margin of the proposed amplifier are shown in Fig. 4. The gain and the phase margin of the circuit are 83.97 dB and 61.68 degrees, respectively. The amplifier's bandwidth is measured to be 3.7MHz. Differential mode and common mode gain are shown at Fig.

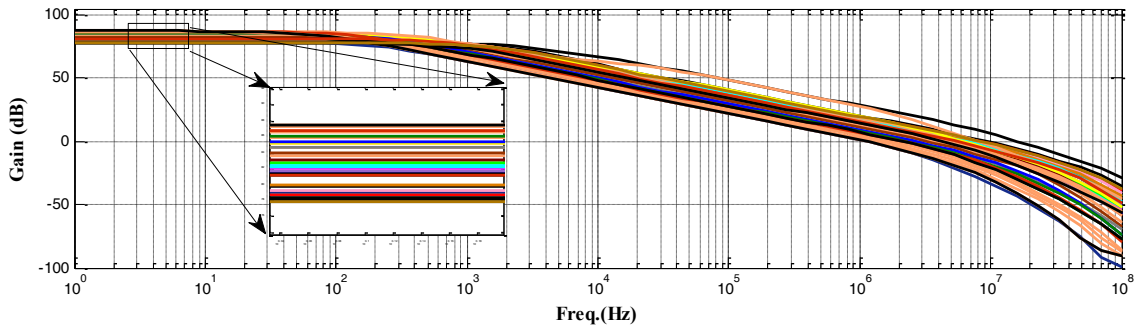


Fig. 7. Monte Carlo analysis for 40 times runs

5. Figure 6 shows the CMRR of the proposed amplifier which is derived almost 90dB

TABLE II PERFORMANCE OF THE OTA UNDER PVT VARIATIONS

parameter		GBW [MHz]	PM [degree]	DC Gain [dB]
corner	FF	3.95	56.4	82.87
	SS	2.8	60.6	83.74
	SF	3.4	62.35	84.15
	FS	3.1	61.23	83.64
	TT	3.7	61.68	83.96
VDD	-10%	3.4	64.2	81.59
	+10%	4.1	58.3	85.12
Temp	-40	3.5	65.4	84.7
	+125	3.9	57.6	82.17

Monte Carlo analysis of amplifier gain with 40 times run is shown at Fig. 7. This analysis verifies the qualitative performance of the proposed amplifier and approves its performance accuracy.

Table I includes the specifications obtained by simulations which is utilized to compare the performance of the proposed amplifier with its other counterparts. Higher gain and CMRR, lower power consumption and bias current and the reliably sufficient phase margin are of the most outstanding features of the proposed circuit. Performance of the OTA under PVT variations are shown at Table II.

IV. Conclusion

In this paper, an amplifier is represented which is based on the CMRR enhancement block. This block eliminates the common mode input and magnifies the differential mode current twice as before and hence increases the DC gain of the amplifier. The proposed amplifier does not require a high supply voltage to provide the optimum performance. Hence, the power consumption is significantly reduced due to low supply voltage along with low bias current incorporated at the amplifier. The suitable specification of the amplifier makes it interestingly suitable for low-voltage, low-power applications.

TABLE III PERFORMANCE SUMMARY AND COMPARISON WITH OTHER WORKS

Parameters	Proposed	[4]	[6]	[18]	[19]	[20]
Technology [µm]	0.18	0.065	0.18	0.35	0.25	-
Supply Voltage [v]	1.5	1.2	1.8	1.5	1.9	±2.5
DC Gain [dB]	83.96	68.9	84.18	82	44.7	82
PM [degree]	61.68	61.0	67.05	86	52	65
GBW [MHz]	3.7	6.4	1.37	1.5	0.81	5
CMRR [dB]	90	-	-	-	88	-
DC Power [µw]	5.949	977.6	19.76	47.25	62	37.8
Bias current [µA]	3.96	814.7	10.4	31.5	32.6	-
Input Voltage Noise @1Hz [$\mu V/Hz^{1/2}$]	4.8	32	31.86	-	-	-
Input Referred Noise [$\mu V/Hz^{1/2}$]	129	-	-	484.7	35	-
C_{load} [pF]	5	5	70	1.2	-	5

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