International Journal Of
Industrial Electronics Control and Optimization
Print ISSN: 3517-2645
Online ISSN: 3568-2645
Homepage: https://ieco.usb.ac.ir/

A Single-Phase Boost AC-AC Converter with Inherent Commutation and Step-Changed Frequency Operation

Babak Fathipour[1] | Ramin Kheyri[1] | Ebrahim Babaei[1] | Samuel Nii Tackie[2]

[1]Faculty of Electrical and Computer Engineering, University of Tabriz, Tabriz, Iran.
[2]Engineering Faculty, Near East University, 99138 Nicosia, North Cyprus, Mersin 10, Turkey
Corresponding author's email: e-babaei@tabrizu.ac.ir

Article Info

Article type:
Research Article

Article history:
Received: 2-February-2025
Received in revised form: 19-May-2025
Accepted: 25-May-2025
Published online:21-March-2026

Keywords:
AC-AC Power Conversion, Inherent commutation, Continuous Input Current, Step-Changed Frequency operation.

ABSTRACT

In this paper, a single-phase boost AC-AC converter with inherent commutation and step-changed frequency operation is proposed. Distinct from conventional AC-AC converters, the proposed design achieves output voltage regulation utilizing one high-frequency switch. The inherent commutation feature of the converter negates the necessity for additional snubber circuits or complex commutation strategies, thereby simplifying the control method for adjusting the output voltage amplitude and frequency. The continuous input current of the proposed converter eliminates the requirement for a bulky LC filter. A straightforward and adaptable switching strategy is implemented to produce output frequency variations. The approach of preventing the conduction of the body diode in power MOSFETs mitigates issues associated with poor reverse recovery, enabling high-speed switching. The operating principles of the converter are elucidated across various modes of operation, with key equations derived and analyzed. To substantiate the validity of the proposed design, simulation results obtained using PSCAD/EMTDC software at frequencies of 25Hz, 50Hz, and 100Hz are presented.

I. Introduction

In various power applications, the demand for reliable and efficient AC-AC power converters is paramount. These converters can be classified into two main categories: indirect and direct AC-AC converters. Indirect AC-AC converters [1, 2], commonly referred to as AC-DC-AC converters, operate through two conversion stages to produce an output waveform with the desired voltage amplitude and frequency. Nonetheless, the process of converting the AC input voltage to a DC voltage, followed by inversion, inevitably introduces harmonic distortion into the power grid. On the other hand, direct AC-AC converters encompass matrix converters [3, 4] and AC-AC pulse width modulation (PWM) converters [5, 6]. Matrix converters are capable of varying both the voltage amplitude and frequency at the output without the need for energy storage components; however, they necessitate the integration of input and output filters and are limited to operating as voltage buck converters. In contemporary power electronic applications, there is an increasing requirement for output voltage boosting. Furthermore, these converters must navigate challenges related to commutation, with a safe commutation strategy proposed in [7] to mitigate such issues. Direct PWM AC-AC converters are often viewed as more suitable for applications where only adjustments to output voltage amplitude are necessary. These converters offer the advantages of single-stage conversion, enhanced efficiency and reliability, and reduced costs [8]. Nevertheless, they are unable to facilitate frequency changes, which have become essential for a wide range of industrial applications. Z-source AC-AC converters are categorized under direct PWM AC-AC converters. Following the introduction of the traditional Z-source inverter (ZSI) in [9], extensive research has been conducted to explore the application of the Z-source network across various power conversion types, including DC-AC [10, 11], AC-DC [12], DC-DC [13, 14], and AC-AC [15], owing to its distinctive features such as boost capability and enhanced reliability compared to voltage source inverters. The initial Z-source AC-AC converter was presented in [15], exhibiting both boost capabilities in-phase and buck/boost functionalities out-of-phase. However, this design was less

reliable than the conventional ZSI, primarily due to the non-ideal characteristics of the complementary bidirectional switches and the inherent delays in their gate drivers. These issues led to unintended overlap or dead times between the switches, resulting in current and voltage spikes, as documented in [16]. Furthermore, the input current in [15] is discontinuous, necessitating the incorporation of an LC filter. A potential solution to the commutation challenges faced by AC-AC converters involves the application of an RC snubber circuit, albeit with significant losses. While the authors of [19, 20] advocate for a complex safe commutation strategy as an alternative to the snubber circuit, this approach is not devoid of shortcomings, as it entails higher costs and increased control complexity. A concept known as "switching cells" was introduced in [17]. This approach involves partitioning the circuit architecture into two identical cells, allowing for the substitution of bidirectional switches with unidirectional switches combined with diodes. To effectively address the commutation challenges posed by the converter using switching cells, precise sensing of the input voltage-particularly in the vicinity of zero-is essential. The modulation of pulse-width modulation (PWM) is dependent on the polarity of the input voltage. Within a switching cell circuit framework, only one high-frequency switch is activated during each half-cycle, with the other remaining inactive until the following half-cycle. If the input voltage polarity is inaccurately sensed, it may result in improper operation of the switches. Therefore, accurate sensing of the input voltage polarity is crucial for the converter's proper functionality. A direct AC-AC converter utilizing four bidirectional power switches was innovated in [18]. This converter features a π-shaped circuit design formed by the power switches and other components, allowing for simultaneous regulation of the output voltage's phase and magnitude. However, it encounters challenges such as commutation difficulties, limited voltage gain, and pulsating input current. Conversely, high-gain Z-source boost AC-AC converters [19, 20] mitigate these issues by implementing a reliable commutation strategy that eliminates the necessity for snubber circuits; however, they do not facilitate inverting operations and involve complex control techniques. Furthermore, a boost AC-AC converter with variable frequency was presented in [21], though it suffers from drawbacks such as the requirement for a bulky input LC filter and low voltage gain. In [22], an asymmetric bipolar output voltage is provided at output. By preventing body diode conduction in MOSFETs, the issues associated with poor reverse recovery are addressed, enabling the implementation of high-speed power MOSFETs. However, the presence of series diodes with all switches increases the total number of semiconductor devices, leading to higher conduction losses and reduced efficiency. In non-inverting operation, the converter can function in boost mode; however, in inverting operation, it is limited to buck-boost mode. This buck-boost operation results in greater voltage and current stresses on the switches compared to boost converters, consequently increasing both switching and conduction losses. While the boost AC-AC converter discussed in [23] facilitates step-changed frequency operation with continuous input current, it is characterized by a low voltage gain. Additionally, this configuration necessitates precise input voltage sensing, which may lead to interface complications in the switches, particularly when the input voltage approaches zero and is not accurately detected. The topology presented in [24] offers both step-changed frequency and bipolar step-up amplitude operations; however, it is hindered by commutation issues and requires dead times between complementary power switches. Furthermore, the inherent connections of the body diodes in the switches contribute to operational challenges. The effective functioning of high-frequency switches in this converter demands exact input voltage sensing, which adds to the complexity of control, increases costs, and contributes to additional losses. In contrast, the converter presented in [25] proposes a single-phase AC-AC configuration that addresses commutation challenges while also ensuring continuous input current. Nevertheless, this design involves a considerable number of high-frequency switches and energy storage components, thereby enhancing its overall complexity. A family of single-phase boost AC-AC converters utilizing impedance network cells with symmetric bipolar operation is introduced in [26]. In this study, output voltage regulation and frequency variation are achieved with the use of only four switches. However, the increased number of diodes results in higher conduction losses, and the input current is quasi-continuous, necessitating the incorporation of a compact input LC filter. The converter outlined in [27] employs switched capacitor cells to achieve high voltage gain; however, it also suffers from commutation challenges, lacks the capability for frequency adjustment, and entails a high number of power switches, ultimately leading to increased implementation costs.

To address the aforementioned challenges, this article proposes a single-phase boost AC-AC converter with inherent commutation and step-changed frequency operation. The proposed converter employs only five switches, which is a reduced count in comparison to other existing converters. In this design, a single high-frequency switch is modulated using a high-frequency PWM signal throughout both half-cycles of the input voltage. This approach obviates the need for precise sensing of input voltage polarity and facilitates the implementation of a straightforward switching strategy. The output frequency can be varied as a multiple or fraction of the input frequency, rendering this converter particularly suitable for applications such as high-gain AC-DC rectifiers, inductive power transmission systems, and traction systems. Unlike indirect AC-DC-AC converters [1, 2], the proposed converter facilitates a single-stage direct AC-AC power conversion and requires only a minimal capacitance of a few microfarads (greater than 1μF). This requirement represents a significant

reduction from the substantially larger dc-link capacitors (greater than 1mF) typically employed in indirect AC-DC-AC converters. As a result, the proposed converter enables the use of a dependable (long lifespan), efficient (characterized by low equivalent series resistance losses), and compact film capacitor.

Moreover, the converter achieves inherent commutation without necessitating the division of the circuit into positive and negative switching cells, thereby enhancing the simplicity of its switching strategy. The input current maintains continuity without the need for a substantial filter on the input side. The prevention of body diode conduction in power MOSFETs mitigates issues related to poor reverse recovery, allowing the use of MOSFETs and enabling selection of a high switching frequency. Consequently, this reduces the size of passive components. The proposed converter has been thoroughly analyzed across various operational modes. To validate the theoretical equations and assess the precision of its performance, simulation results obtained using PSCAD/EMTDC software are presented.

II. Proposed Single-phase AC-AC Converter

The configuration of the proposed AC-AC converter is illustrated in Fig. 1. This converter comprises one high-frequency switch (S), four low-frequency switches (S_1, S_2, S_3, S_4), one inductor (L), seven diodes (D_{p1}, D_{p2}, D_{n1}, D_{n2}, D_1, D_2, D_3), and three capacitors (C_1, C_2, C_3). The low-frequency switches determine the output voltage polarity in relation to the input voltage source (v_i), allowing operations in both non-inverted and inverted modes. Capacitors are integrated into the design to store energy and provide a freewheeling path for the current flowing through the inductor, thereby enabling the proposed AC-AC converter to utilize an inherent commutation strategy. Consequently, there is no requirement for an additional safe commutation strategy or snubber circuit.

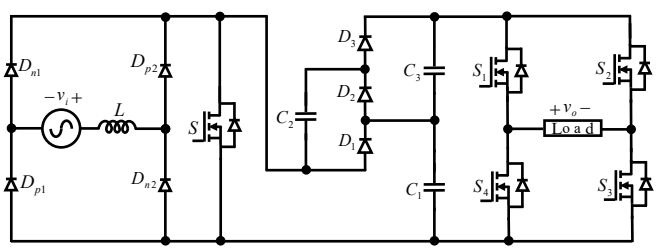


Fig. 1. The configuration of the proposed converter.

A. Switching Strategies of proposed converter

Fig. 2 illustrates the switching strategy employed by the proposed AC-AC converter to generate three distinct output frequencies: $f_i/2$, f_i, and $2f_i$. As depicted, the colored waveforms of the output voltage enhance the interpretation of states 1, 2, 3, and 4 across the various frequencies. These states (1-4) are determined by the conditions of the positive and negative input voltage sources during each half-cycle and the activation of the positive switch pairs (S_1, S_3) and negative switch pairs (S_2, S_4). State 1 is realized when the input voltage source is within its positive half-cycle and is conveyed to the output via the positive switch pairs, resulting in an in-phase output, referred to as non-inverting. In contrast, state 2 is achieved when the input voltage remains in its positive half-cycle and the negative switch pairs are engaged, leading to an out-of-phase output, thus termed inverting. States 3 and 4 occur during the negative half-cycle of the input voltage, depending on whether S_1 and S_3 or S_2 and S_4 are activated, resulting in inverting and non-inverting configurations with respect to the output, respectively. These four states facilitate the generation of varying output frequencies. The proposed converter is capable of producing frequencies $f_o=kf_i$ and $f_o=f_i/k$ where k=1,2, 3, … at the output.

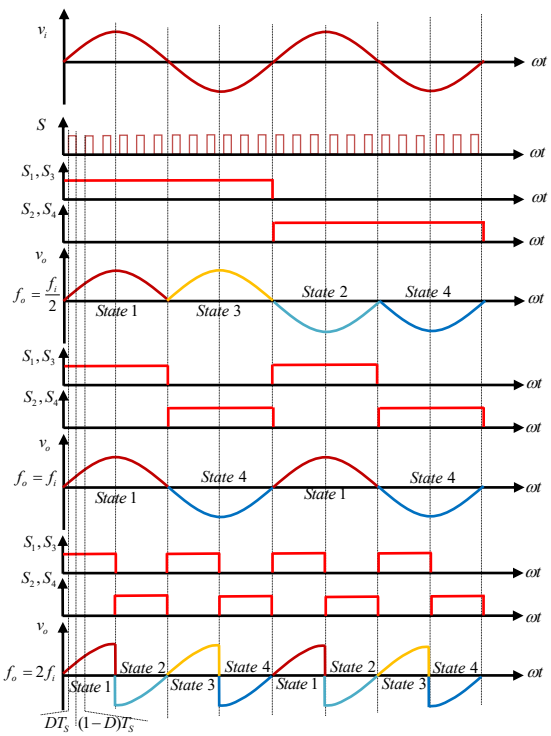


Fig. 2. The switching strategy of the proposed converter.

B. Analysis of proposed converter

The proposed AC-AC converter is examined in two operational states: state 1, characterized by a positive input and a corresponding positive output, and state 4, marked by a negative input producing a negative output, for the purpose of generating an output frequency of $f_o=f_i$. Similarly, an analysis of the converter in states 2 and 3 can be conducted to yield frequencies of $f_o=f_i/2$ and $f_o=2f_i$. The converter has been studied in two distinct operational modes: DT_s and $(1-D)T_s$ intervals. Key equations have been established concerning the voltage stress experienced by components, the current flowing through them, and the voltage gain of the converter. Prior to the analysis, the following assumptions are made: 1) The converter operates under continuous conduction mode; 2) The switching

frequency (f_s) is significantly greater than the input source frequency (f_i); and 3) All components are treated as ideal.

State 1: In state 1, the positive switch pairs S_1 and S_3 are activated, while switches S_2 and S_4 remain in the off position, resulting in non-inverting operation. During the positive half-cycle of the input voltage, diodes D_{p1} and D_{p2} are conducting, whereas diodes D_{n1} and D_{n2} are non-conductive in this state. The switch S operates during the intervals defined by DT_s and (1-D)T_s; as previously mentioned, switch S remains active throughout both half-cycles of the input voltage.

***DT*$_s$ interval:** Fig. 3(a) illustrates the equivalent circuit for this operational mode. The switch S is activated during the DT_s interval. The diodes D_1 and D_3 remain non-conductive due to the negative voltage present across them, resulting in the creation of a parallel configuration involving capacitors C_1, D_2, C_2, and S. Initially, the inductor L is charged through a loop that comprises the input voltage source, D_{p1}, D_{p2} and S, leading to an increase in the energy stored in the inductor. Subsequently, capacitor C_2 is charged via the established parallel loop, causing its voltage to rise. Ultimately, the voltage across capacitors C_1 and C_3 provides power to the load. The application of KVL in this operational mode can be expressed as follows:

$$v_L = v_i \tag{1}$$

$$v_{C1} = v_{C2} \tag{2}$$

$$v_o = v_{C3} + v_{C1} \tag{3}$$

(1-*D*)*T*$_s$ interval: Referring to the equivalent circuit depicted in Fig. 3(b), the S is turned off, resulting in D_2 not conducting during the interval of (1-D)T_s. C_1 is charged by the input voltage and L through the loop formed by D_1, D_{p1} and D_{p2}, leading to an increase in the energy stored within the C_1. Additionally, C_3 is charged by capacitor C_2. By applying KVL in this operational mode, the equation can be derived as follows:

$$v_L = v_i - v_{C1} \tag{4}$$

$$v_{C2} = v_{C3} \tag{5}$$

By employing the voltage-second balance principle for inductor L, the voltage across the capacitors can be expressed as follows:

$$v_{C1-C3} = +\frac{v_i}{1-D} \tag{6}$$

By substituting equation (6) into equation (3), the voltage gain (G) of the proposed converter in state 1 is derived as follows:

$$G = \frac{v_o}{v_i} = +\frac{2}{1-D} \tag{7}$$

State 4: In state 4, the negative switch pairs S_2 and S_4, along with D_{n1} and D_{n2}, are activated during the negative half-cycle of the input voltage source, facilitating non-inverting operation.

***DT*$_s$ interval:** The equivalent circuit for this operational mode is presented in Fig. 3(c). During this mode, the S is activated. Diodes D_1 and D_3 are reverse biased and do not conduct. The energy stored in the inductor L is increased through a loop that comprises the input voltage source, D_{n1}, D_{n2} and S. The energy stored in capacitor C_1 also serves to charge capacitor C_2, while the load is supplied by capacitors C_1 and C_3. The application of KVL in this operational mode can be expressed as follows:

$$v_L = v_i \tag{8}$$

$$v_{C1} = v_{C2} \tag{9}$$

$$v_o = v_{C3} + v_{C1} \tag{10}$$

(1-*D*)*T*$_s$ interval: The equivalent circuit for this mode is illustrated in Fig. 3(d). The S is deactivated during in (1-D)T_s interval. C_1 is charged via the loop formed by the input voltage source v_i, L, D_{n1}, D_{n2}, and D_1. With a positive voltage applied across D_1, and D_3, these diodes become conductive, providing a pathway for the energy stored in the inductor L to discharge into C_1, C_3, and the load. The application of KVL in this operational mode can be articulated as follows:

$$v_L = v_i - v_{C1} \tag{11}$$

$$v_{C2} = v_{C3} \tag{12}$$

By employing the voltage-second balance principle for inductor L, the voltage across the capacitors in state 4 can be expressed as follows:

$$v_{C1-C3} = +\frac{v_i}{1-D} \tag{13}$$

By substituting equation (13) into equation (10), the voltage

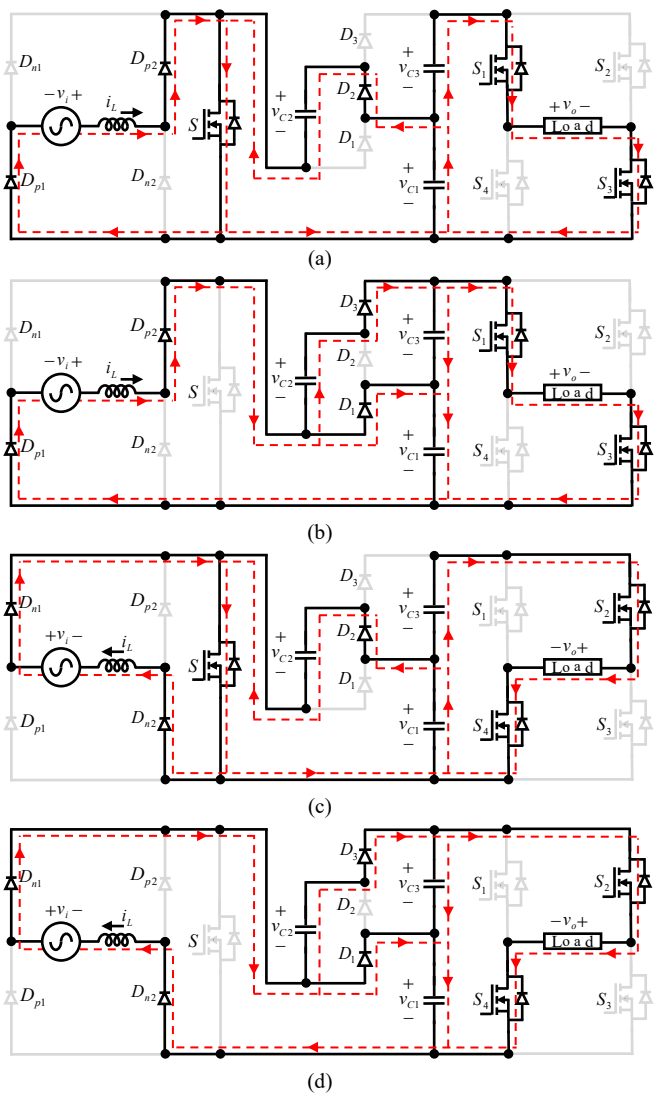


Fig. 3. Equivalent circuits of the proposed converter (a) DT_s interval of state 1. (b) (1-D)T_s interval of state 1. (c) DT_s interval of state 4. (d) (1-D)T_s interval of state 4.

gain of the proposed converter in state 4 is derived as follows:

$$G = \frac{v_o}{v_i} = +\frac{2}{1-D} \quad (14)$$

Based on the equations presented in equation (7) and equation (14), when the signs of the input voltage and output voltage are identical (either both positive or both negative) during a half-cycle, the voltage gain is positive (as seen in states 1 and 4). This indicates a non-inverting output relative to the input voltage. Conversely, when the input voltage is positive while the output voltage is negative, or vice versa (as observed in states 2 and 3), the voltage gain exhibits a negative sign, indicating that the output is inverted in relation to the input voltage.

III. Parameter Design

A. Active Components Selection

Semiconductor devices must be selected to withstand the maximum peak voltage and current values without sustaining damage. Therefore, it is imperative to ascertain the maximum voltage and current specifications for the switches and diodes. The peak voltage stresses experienced by the switches and diodes can be calculated using the following equations:

$$\begin{cases} V_{S(peak)} \\ V_{D1-D3(peak)} \\ V_{D1p,n(peak)} \\ V_{D2p,n(peak)} \end{cases} = \sqrt{2}\frac{1}{(1-D)}V_{i(rms)} \qquad V_{S1-S4(peak)} = \sqrt{2}\frac{2}{(1-D)}V_{i(rms)} \quad (15)$$

The peak current flowing through the switches, diodes, and inductor, as well as the root mean square (RMS) currents of the switches, inductor, and capacitors, and the average currents of the switches and diodes over a complete line cycle are calculated and presented in Table 1.

TABLE 1: THE CURRENT EQUATIONS OF COMPONENTS

Switches/$I_{o(rms)}$		
Peak	RMS	Average
$\boldsymbol{I_S = \frac{\sqrt{2}(1+D)}{D(1-D)}}$	$I_S = \frac{1+D}{(1-D)\sqrt{D}}$	$I_S = \frac{2\sqrt{2}(1+D)}{\pi(1-D)}$
$\boldsymbol{I_{S3-S6} = \sqrt{2}}$	$I_{S1-S4} = \frac{1}{\sqrt{2}}$	$I_{S1-S4} = \frac{\sqrt{2}}{\pi}$
Diodes/$I_{o(rms)}$		
Peak		Average
$\boldsymbol{I_{\substack{D1p,n \\ D2p,n}} = \frac{2\sqrt{2}}{(1-D)},\ I_{D1,D3} = \frac{\sqrt{2}}{(1-D)}}$		$I_{\substack{D1p,n \\ D2p,n}} = \frac{2\sqrt{2}}{\pi(1-D)},\ I_{D1-D3} = \frac{2\sqrt{2}}{\pi}$
$\boldsymbol{I_{D2} = \frac{\sqrt{2}}{D}}$		
Inductor/$I_{o(rms)}$		
Peak		RMS
$\boldsymbol{I_L = \frac{2\sqrt{2}}{(1-D)}}$		$I_L = \frac{2}{(1-D)}$
Capacitors/$I_{o(rms)}$		
RMS		
$\boldsymbol{i_{C1} = \frac{(1+D)}{\sqrt{D(1-D)}},\ i_{C2} = \sqrt{\frac{1}{D(1-D)}},\ i_{C3} = \sqrt{\frac{D}{1-D}}}$		

B. Passive Components Design

The required inductance value can be determined using the following equation:

$$L = \frac{|V_L|DT_S}{|\Delta I_L|} \quad (16)$$

In the previous equation, the voltage applied across the inductor during $\Delta T = DT_S$ is represented by $|V_L|$. The maximum permissible current ripple, denoted as ΔI_L, has been established as $\Delta I_L = x\%I_{L(peak)}$, where $I_{L(peak)}$ represents the peak current stress experienced by the inductor, as indicated in Table 1. Consequently, the necessary inductance value for the proposed converter can be derived using the following equation:

$$L = \frac{DV_{i(rms)}^2}{x\%f_sP_o} \quad (17)$$

The required capacitance value is determined through a methodology analogous to that used for calculating inductance values. Consequently, the necessary capacitance can be expressed as follows:

$$C = \frac{|I_C|DT_S}{|\Delta V_C|} \quad (18)$$

In this context, $|I_C|$ represents the current flowing the capacitor during the DT_s interval, $\Delta V_C = y\%V_{C(peak)}$ denotes the maximum permissible voltage ripple, and $V_{C(peak)}$ signifies the peak voltage across the capacitor. Therefore, the necessary capacitance value for the proposed converter can be computed as follows:

$$\begin{cases} C_1 = \frac{(1+D)(1-D)^2P_o}{2y\%f_sV_{i(rms)}^2} \\ C_2 = \frac{(1-D)^2P_o}{2y\%f_sV_{i(rms)}^2} \\ C_3 = \frac{D(1-D)^2P_o}{2y\%f_sV_{i(rms)}^2} \end{cases} \quad (19)$$

IV. Control Block Diagram for Output Voltage Regulation

The control block diagram for the proposed converter is shown in Fig. 4. In order to regulate the operation of the switch pairs S_1,S_3 and S_2,S_4, which operate at line frequency, a comparator is employed to assess the polarity of the input voltage. The peak output voltage is calculated using the methodology outlined in [29], as illustrated in the block diagram in Fig. 5, and is acquired as follows:

$$\sqrt{[v_o\,sin(\omega t)]^2 + [v_o\,cos(\omega t)]^2} = V_{o(peak)} \quad (20)$$

The incorporation of low-pass filters (LPFs) at both inputs of the peak voltage detector is intended to attenuate high-frequency noise, thereby decreasing the potential for erroneous switch activations. The detected peak output voltage ($V_{o(peak)}$) is then compared to the reference voltage ($V_{o(ref)}$), resulting in the generation of an error signal ($v_e(t)$). This error signal is processed by a proportional-integral (PI) controller, which computes the duty cycle ($D(t)$) necessary to adjust the output voltage to the desired reference level. The operation of the PI controller is characterized by the

proportional gain (k_p) and the integral gain (k_i), as depicted in Fig. 4. Ultimately, the control signals consist of a high-frequency PWM pulse for switch S, in addition to four low-frequency PWM pulses (operating at line frequency) for switches S_1-S_4, which are subsequently sent to the converter.

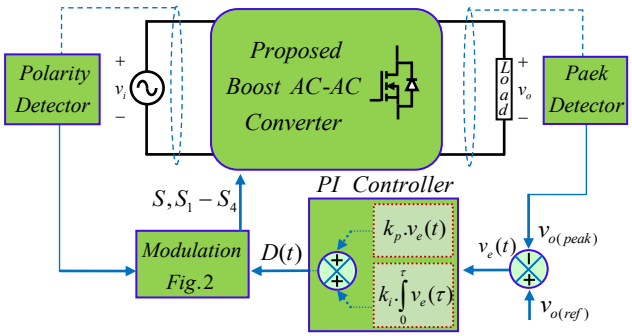


Fig. 4. The control block diagram of the proposed converter.

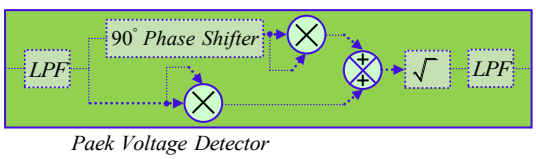


Fig. 5. The block diagram of the peak voltage detector.

V. Comparative Analysis

Table 2 presents a comparative analysis between the proposed converter and various other single-phase boost AC-AC converters. The voltage gain relative to the duty cycle for the proposed converter, alongside the gains of other converters, is illustrated in Fig. 6(a). The voltage gain of the proposed converter is found to be comparable to that of the converter presented in [27], while exceeding the gains of most other converters. As shown in Table 2, the proposed topology features the fewest switches in its design, second only to the converter in [26], which utilizes four active switches but additionally requires nine external diodes and exhibits a discontinuous input current. Moreover, converters [20, 24, 27] face commutation issues that necessitate dead or overlap times to avoid short circuits in capacitors and open circuits in inductors, negatively impacting the quality of the output voltage waveform. Although the converter discussed in [25] addresses commutation challenges, it does so at the cost of employing a significant number of active and passive components while yielding a low voltage gain. The proposed converter, along with those in [23-26], provides symmetrical voltage gain and enables step-changed frequency operation, making them particularly suitable for high-gain AC-DC rectifiers and traction systems. The converters detailed in [20] and [22-27] depend on precise input voltage polarity sensing, as the operation of their high-frequency switches is contingent upon accurate detection of this polarity. Such dependence can lead to interface complications, especially when the input voltage is close to zero and its polarity cannot be precisely identified. In contrast, the proposed converter mitigates this issue by employing a single high-frequency switch that operates across both half-cycles of the input voltage, independent of voltage polarity sensing. Furthermore, converters [20, 24, 27] experience challenges due to high-frequency conduction of the body diode in the switching devices, along with associated reverse recovery problems.

Fig. 6(b) and 6(c) illustrate a reduction in both the total voltage stress across the switches and the current that flows through them in the proposed converter. While converters [20, 22, 26, and 27] also exhibit reductions in voltage stress for various voltage gains (G) when compared to the proposed converter, they are associated with significant issues, including commutation challenges, increased complexity in control and switching patterns, a higher number of high-frequency switches, and conduction through the body diode of the switching devices. The switching device peak power (SDP_{peak}), which is directly correlated to the overall power rating and cost of the switching devices, as well as the average power (SDP_{ave}), which is related to losses and the thermal requirements of the devices [28], are defined for the proposed converter as follows:

$$SDP_{peak} = \sum_{n=1}^{N} V_{n(peak)} I_{n(peak)} = \frac{2+18D-8D^2}{D(1-D)} P_o \quad (21)$$

$$SDP_{ave} = \sum_{n=1}^{N} V_{n(peak)} I_{n(ave)} = \frac{24-12D}{\pi(1-D)} P_o \quad (22)$$

In equations (21) and (22), $V_{n(peak)}$, $I_{n(peak)}$, and $I_{n(ave)}$ represent the peak voltage, peak current, and average current of the *nth* device, respectively. The normalized values for peak power (SDP_{peak}) and average power (SDP_{ave}) of both the proposed converter and its counterparts are presented in Fig. 7 as a function of voltage gain. It is evident that the proposed converter demonstrates the lowest peak and average power ratings for the switching devices when compared to converters [20, 22, 23, 25, 26]. This suggests that the proposed converter requires a reduced total power rating, lower cost, diminished losses, and minimized heatsink requirements.

VI. Simulation Results and Loss Analysis

A. Simulation Results

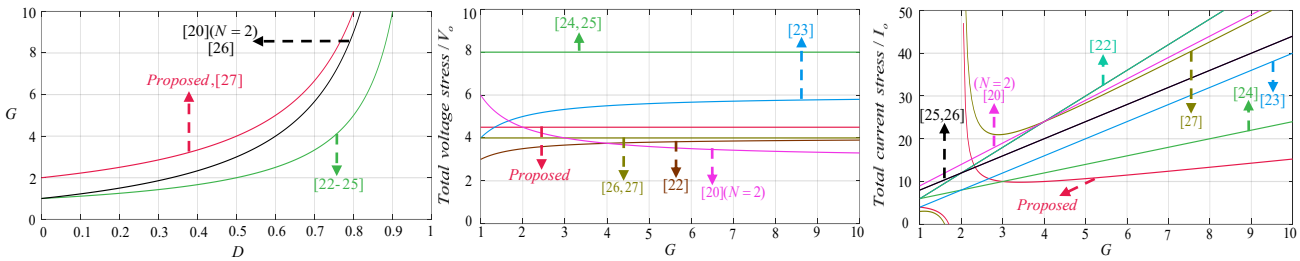
To validate the effectiveness and ensure the reliability of the proposed converter, simulation results are presented using PSCAD/EMTDC software. The parameters employed in the simulation are outlined in Table 3. To demonstrate the capability of the proposed converter regarding step-changed frequency operation, performance evaluations have been conducted at three specific frequencies: 25Hz (stepped down), 50Hz (identical to the input voltage source), and 100Hz (stepped up), with a duty cycle (D) of 0.5. Fig. 8(a) illustrates the input voltage waveform (V_i), which exhibits a peak value of

TABLE 3: PARAMETERS USED IN THE SIMULATION

Parameters and Values						
$V_{i(peak)}$	f_S	D	f_i	$C_1 - C_3$	L	$load$
50 V	100KHZ	0.5	50HZ	4μF	400μH	80Ω

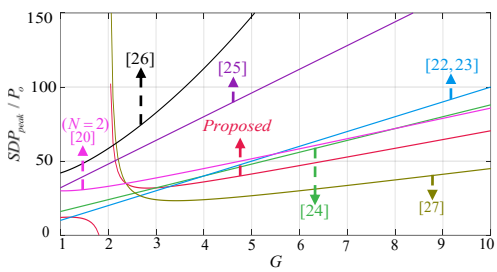
TABLE 2: COMPARISON OF THE PROPOSED CONVERTER WITH OTHER AC-AC CONVERTERS

Parameters	[20]	[22]	[23]	[24]	[25]	[26]	[27]	Proposed
Voltage gain	$\frac{1+(N-1)D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{2}{1-D}$	$\frac{2}{1-D}$
No. of switches	4	6	6	8	8	4	8	5
No. of diodes	-	6	8	-	8	9	-	7
No. of inductors	1	1	1	2	6	2	1	1
No. of capacitors	2	2	2	3	3	1	3	3
Symmetrical voltage gain	No	No	Yes	Yes	Yes	Yes	No	Yes
Continuous input current	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes
Step-changed frequency operation	No	No	Yes	Yes	Yes	Yes	No	Yes
Control complexity	High	Moderate	Moderate	Moderate	Moderate	Moderate	High	Low
Inherent commutation	No	Yes	Yes	No	Yes	Yes	No	Yes
Need dead or overlap time	Yes	No	No	Yes	No	No	Yes	No
Body diodes conduction	Yes	No	No	Yes	No	No	Yes	No

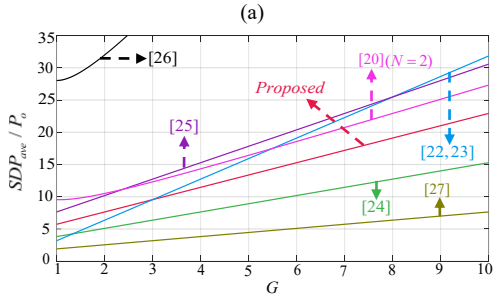


(a) (b) (c)

Fig. 6. Comparison plots, (a) Voltage gain, (b) Total switches voltage stress, (c) Total switches current stress.



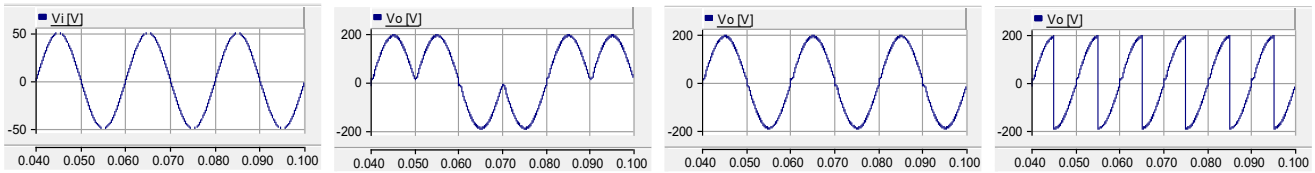
(a)



(b)

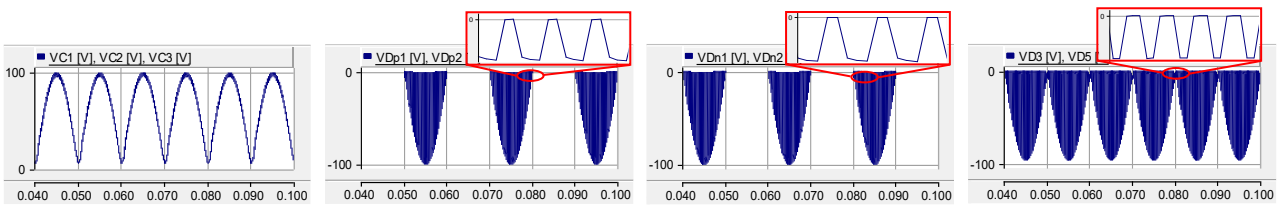
Fig. 7. Total switching devices power of the proposed converter and other converters, (a) SDP_{peak}. (b) SDP_{ave}.

$50V$. Fig. 8(b) presents the output voltage waveform (V_o) of the proposed converter at $25Hz$, revealing four distinct states corresponding to the signs of the input voltage source. The output voltage waveform (V_o) for the frequency of $50Hz$ is depicted in Fig. 8(c), where it can be observed that the output voltage is increased and remains entirely in phase with V_i. Based on equation (7), the maximum output voltage is calculated to be $200V$, which aligns well with the simulation results obtained. Subsequently, Fig. 8(d) shows the output voltage waveform of the proposed converter at f_o=$100Hz$, which also exhibits four states. As illustrated in Fig. 8(d), each half-cycle of the input voltage contains two states, which are either inverted or non-inverted based on the sign of the input voltage. The voltage stress on the capacitors, switches, and diodes with their zoomed-in waveforms is depicted in Figs. 9(a) to 10(d). The calculated voltage stress values on the capacitors, derived from (6), and those on the switches and diodes, calculated using (15), closely correlate with the simulation outcomes presented in Figs. 9(a) to 10(d). The zoomed-in waveforms illustrating the voltage stress across the semiconductors indicate the absence of short circuits or voltage spikes during the operation of the proposed converter, which is consistent with the analytical results obtained. Fig 11(a) and Fig. 11(b) presents the simulation results for the input and output voltage and current waveforms, along with their zoomed-in views, under an R-L load characterized by a resistance of R=80Ω and inductance L=$50mH$, operating at an output of $50Hz$.



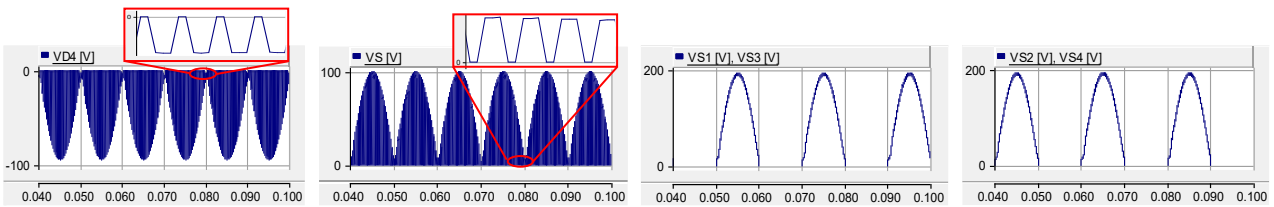
(a) (b) (c) (d)

Fig. 8. Simulation results of input and output waveforms for step-changed frequency operation. (a) Input voltage. (b) Output voltage for 25Hz. (c) Output voltage for 50Hz. (d) Output voltage for 100Hz.



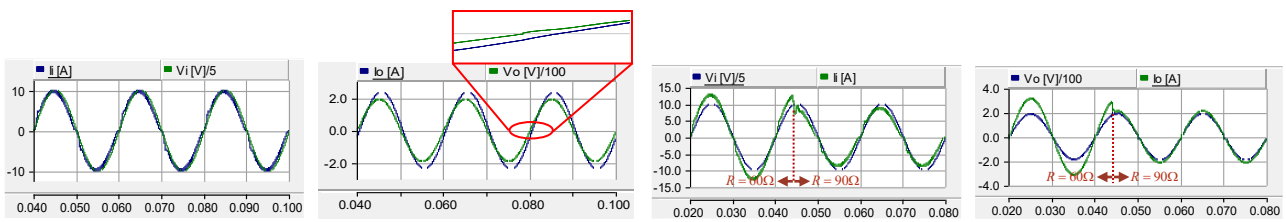
(a) (b) (c) (d)

Fig. 9. Simulation results of voltage stress waveforms. (a) Across capacitors. (b) Across D_{p1}, D_{p2}. (c) Across D_{n1}, D_{n2}. (d) Across D_3, D_5.



(a) (b) (c) (d)

Fig. 10. Simulation results of voltage stress waveforms. (a) Across D_4. (b) Across S. (c) Across S_1, S_3. (d) Across S_2, S_4.



(a) (b) (c) (d)

Fig. 11. Simulation results, (a) Input waveforms under RL load, (b) Output waveforms under RL load, (c) Input waveforms under transient load, (d) Output waveforms under transient load.

This demonstrates the proposed converter's capability to manage non-unity load conditions. Additionally, the input and output waveforms of the proposed converter are depicted in Figs. 11(c) and 11(d), showcasing its performance as the load resistance varies from 60Ω to 90Ω. The waveform analysis reveals the converter's proficiency in sustaining inherent commutation while exhibiting the absence of voltage spikes during load transitions.

B. Loss Analysis

In non-ideal operating conditions, each component of the converter contributes to the overall power losses. These losses are primarily categorized into two types: conduction loss (P_{cond}) and switching loss ($P_{switching}$), which together constitute the total power loss of the converter (P_{Loss}). To obtain an accurate assessment of the total losses, it is essential to consider several key parameters, including the on-state resistance of the switches (r_S), the equivalent series resistance associated with the capacitors (r_C), the resistance of the inductor (r_L), the forward voltage drops across the diodes (V_F), the switching frequency (f_s), as well as the turn-on (t_r) and turn-off (t_f) times of the switches. The formulations for P_{cond}, $P_{switching}$, and P_{Loss} can be expressed as follows:

$$\begin{cases} P_{cond} = r_S(I^2_{S(rms)} + I^2_{S1-S4(rms)}) + r_L(I^2_{L(rms)}) + \\ V_F(I_{D1p,n(ave)} + I_{D3-D5(ave)}) + \\ \quad D2p,n(ave) \\ r_C(I^2_{C1(rms)} + I^2_{C2(rms)} + I^2_{C3(rms)}) \\ P_{switching} = \frac{1}{6} V_{S(rms)} I_{S(rms)} f_s (t_r + t_f) \\ P_{Loss} = P_{cond} + P_{switching} \end{cases} \quad (23)$$

It is presumed that the voltage and current fluctuations in the inductors and capacitors are insignificant. The switching losses are primarily associated with the high-frequency switch S. The

root mean square (RMS) values of the currents flowing through the capacitors, inductors, and switches, along with the average current values for the diodes, are computed over one line period and presented in Table 2. This can be formally expressed as follows:

$$\begin{cases} P_{Loss} = r_S\left[\left(\frac{1+D}{(1-D)\sqrt{D}}\right)^2 + \left(\sqrt{2}\right)^2\right] I_{o(rms)}^2 + \\ \frac{1}{6} V_{S(rms)} I_{S(rms)} f_S (t_r + t_f) + \\ V_F\left(\frac{8\sqrt{2}}{\pi(1-D)} + \frac{6\sqrt{2}}{\pi}\right) I_{o(rms)} + r_L\left(\frac{2}{1-D}\right)^2 I_{o(rms)}^2 + \\ r_C\left[\left(\frac{1+D}{\sqrt{D(1-D)}}\right)^2 + \left(\sqrt{\frac{1}{D(1-D)}}\right)^2 + \left(\sqrt{\frac{D}{1-D}}\right)^2\right] I_{o(rms)}^2 \end{cases} \quad (24)$$

Ultimately, the efficiency of the proposed converter can be evaluated as follows:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \quad (25)$$

The non-ideal voltage gain (G') of the proposed converter can be expressed using the following equation:

$$G' = \frac{G}{1+(P_{Loss}/P_o)} \quad (26)$$

Fig. 12 presents the characteristics of conversion efficiency and voltage gain as a function of duty cycle (D) under the specified conditions: $v_{i(rms)}$=50V, V_F=0.7V, r_S=0.04Ω, t_r+t_f=100ns, f_s=100kHz, and R=80Ω. The analysis in Fig. 12 indicates that at high duty cycles, an increase in inductor resistance (r_L) and capacitors resistance ($r_{C1} = r_{C2} = r_{C3} \approx r_C$) can significantly impair both the voltage gain and efficiency of the converter.

Fig. 13 presents a comparison of the efficiency curves for the proposed converter alongside those of other converters [20, 22, 23, 26] under matched operating conditions, specifically at an output voltage of 140V_{rms} and a gain of 4, over a broad spectrum of output powers ranging from 50W to 450W. As depicted in Fig. 13, the proposed converter exhibits superior efficiency compared to the other converters throughout the entire output power range. The impressive efficiency attained by the proposed converter can be attributed to several factors, including the optimized use of a reduced number of switches

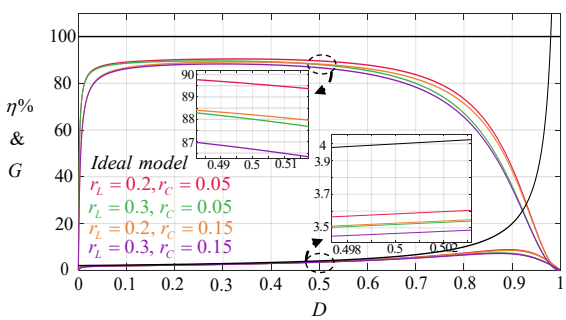


Fig. 12. The efficiency and non-ideal voltage gain curves.

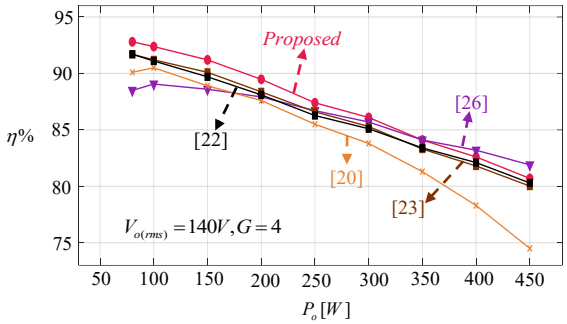


Fig. 13. The efficiency of the proposed converter.

and the effective mitigation of commutation issues, achieved without any overlap or dead time.

VII. Conclusion

This paper presents a single-phase boost AC-AC converter with inherent commutation and step-changed frequency operation. When compared to existing boost AC-AC converters, the proposed design exhibits a higher voltage gain and eliminates the necessity for bidirectional switches. Moreover, the commutation issue is addressed inherently, negating the need for division into two sub-circuits, which effectively reduces the number of components, overall costs, and size of the converter. As illustrated in Fig. 2, the proposed converter features a straightforward control method that involves turning a single high-frequency switch on and off during both half-cycles of the input voltage. This configuration helps minimize conduction losses and enhance overall efficiency. The simulation results validate these assertions across three frequencies: 25Hz, 50Hz, and 100Hz.

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Babak Fathipour was born in Tabriz, Iran, in 1999. He received a B.Sc. degree in Electrical Power Engineering, and an M.Sc. degree in Power Electronics Engineering from University of Tabriz, Tabriz, Iran in 2021 and 2023, respectively. His current research interests include power electronic converters and renewable energy systems.

Ramin Kheyri received his B.Sc. in Electrical Engineering from Urmia University of Technology in 2006, his M.Sc. in Electrical Engineering from the University of Science and Research in 2009, and his Ph.D. in Electrical Engineering from Shahrood University of Technology in 2023. Dr. Kheyri's areas of interest include: Power Electronics, Power Electronics Control, Power Electronic Converters, Power Electronic Converter Modeling, and Electrical Energy Generation.

Ebrahim Babaei (M'10, SM'16) received the Ph.D. degree in Electrical Engineering from the University of Tabriz, in 2007. He is the author and co-author of one book and more than 720 journal and conference papers. He also holds 26 patents in the area of power electronics. His current research interests include the analysis, modelling, design, and control of Power Electronics Converters and their applications, Renewable Energy Sources, and FACTS Devices.Prof. Babaei has been the Editor-in-Chief of the Journal of Electrical Engineering of the University of Tabriz, since 2013. He was an Associate Editor of the IEEE Transactions on Industrial Electronics from 2015 to 2023. He is also currently an Associate Editor of the IEEE Transactions on Power Electronics, IEEE Open Journal of the Industrial Electronics Society, Iranian Journal of Science and Technology, Transactions of Electrical Engineering, and International Journal of Circuit Theory and Applications. He was selected by the Ministry of Science Research and Technology as the distinguished researcher of Iran in the field of engineering in 2022.

Samuel Nii Tackie received his MSc and PhD in Electrical and Electronic Engineering from Near East University in 2015 and 2021, respectively. He has a solid, young, demonstrable profession in both academia and engineering, incorporating teaching, research, supervision, and hands-on practice to advance the field of electrical and electronic engineering. Currently, his research area of interest includes: Power Electronics, Renewable Energy Sources, Generation of Electrical Energy, Custom Power Devices, and Power Electronic Converters.