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A New Quadratic Voltage Lift Cascaded Boost Topology for Hydrogen Extraction

Mohammad Reza Shaker Ardakani[1,2] | Sara Hasanpour[3]* | Majid Moazzami[1,2] | Fariborz Haghighatdar Fesharaki[1,2] | Mahnaz Hashemi[1,2]

Department of Electrical Engineering, Na.C., Islamic Azad University, Najafabad, Iran.[1]
Smart Microgrid Research Center, Na.C., Islamic Azad University, Najafabad, Iran.[2]
Department of Electrical Engineering, Ram.C., Islamic Azad University, Ramsar, Iran.[3]
Corresponding author's email: Sara.Hasanpour@iau.ac.ir

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ABSTRACT

This paper presents a novel non-isolated DC-DC converter topology with several significant advantages. First, the input current remains continuous, thereby reducing the current stress on the input filter capacitor. Second, the converter utilizes the same number of inductors as conventional topologies such as SEPIC, Zeta, and Ćuk converters. Third, it achieves high voltage gain at relatively low duty cycles. Fourth, the maximum voltage stress on the semiconductors remains well below the output voltage, ensuring improved device reliability. Fifth, the design incorporates only a single switch, simplifying the drive circuitry. Sixth, the voltage stress on the switch is significantly lower than the output voltage. Seventh, a quadruple voltage-lift is realized using an enhanced diode–capacitor voltage multiplier integrated at both stages of the converter. Finally, although the power circuit employs 15 diodes and 14 capacitors, the topology maintains a high voltage gain density, justifying the component count. Experimental results are provided to validate the theoretical analysis. The implemented prototype successfully boosts an input voltage of 20 V to an output of 1200 V at a 50% duty cycle, delivering an output power of less than 200 W.

I. Introduction

Hydrogen is widely recognized as a clean and sustainable energy source for the future [1]. It can be efficiently extracted from water, a resource that covers the majority of Earth's surface [2], [3]. Although water electrolysis can occur at low voltages, applying high-voltage pulses with a low average value has been shown to significantly enhance hydrogen production efficiency due to kinetic and ohmic losses [4], [5]. High voltage enables rapid gas output in a given cell, which is crucial for applications demanding high throughput or compact system size. High voltage can forcibly drive a substantial current even in systems with high internal resistance (e.g., cells with large electrode gaps, low-conductivity electrolytes, or resistive solid electrolytes). Low-voltage DC sources such as batteries, fuel cells, and photovoltaic (PV) panels are readily available [6]-[8]. However, their output voltages are typically insufficient to drive the input terminals of pulse power converters used in high-efficiency water electrolysis systems [9], [10]. Therefore, a high-gain DC-DC conversion stage is essential. Transformer-based DC-DC converters are one possible solution [11], [12]. However, high-frequency transformers increase the overall system cost, size, weight, electromagnetic interference (EMI), and voltage stress on semiconductors [13], [14]. As electrical isolation is not always required in these applications, non-isolated high-gain DC-DC converters offer a more compact and cost-effective alternative [15].

Among non-isolated converter topologies, the conventional boost converter (Fig. 1(a)) remains the most widely adopted due to its simplicity, compactness, and reliability. However, its voltage gain is inherently limited, making it unsuitable for high-voltage applications. One common approach to enhance its performance is by integrating diode–capacitor voltage

multiplier cells, as illustrated in Figs. 1(b) and 1(c). These configurations utilize the voltage-lift technique to boost the output voltage. Nevertheless, the resulting voltage gain is typically limited to only twice that of the conventional boost converter. Another method to achieve higher voltage gain is through the cascaded boost converter topology (Fig. 1(d)), which provides a quadratic voltage gain relative to the original boost converter. Despite this improvement, the topology requires duty cycles greater than 50% to surpass the gain achieved by modified boost structures. Additionally, it suffers from a major drawback: the voltage stress on the switch equals the full output voltage, which can reduce reliability and increase cost. The topology shown in Fig. 1(e) addresses the issue of switch voltage stress; however, it still falls short in achieving sufficiently high voltage gain for demanding applications.

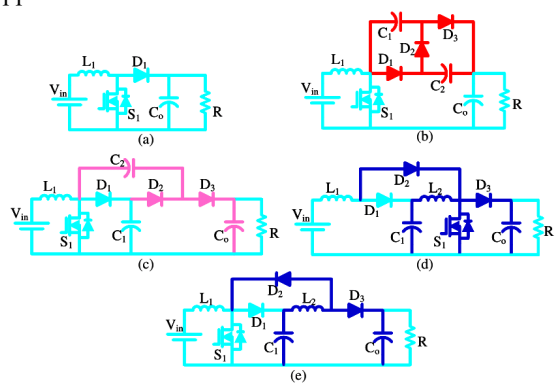


Fig. 1. The classic boost topology. (a) Classic boost converter, (b) and (c) Boost converter using diode–capacitor voltage multiplier cells, (d) Classic quadratic converter, and (e) Boost converter with reduced voltage stress.

The topologies proposed in [16]–[48] represent various improved non-isolated DC-DC converters. Among these, the structures presented in [16]–[20] offer multi-mode operation, functioning as step-up, step-down, and pass-through converters. However, they require relatively high duty cycles to achieve voltage gains exceeding that of the conventional boost converter. Additionally, the voltage stress on the semiconductors in these designs often exceeds the output voltage, which is generally undesirable for practical applications.

The converters introduced in [21]– [22] exhibit improved voltage gain compared to those in [16]– [20], yet they suffer from the same drawbacks—namely, high voltage stress and dependency on large duty cycles. Similarly, the topologies described in [23]– [25] offer marginally better voltage gain but continue to exhibit the aforementioned limitations. Furthermore, they introduce an additional issue: reversed output polarity, which complicates integration with standard loads.

The quadratic boost topologies in [26]–[27] achieve better voltage gains than the aforementioned designs. However, their performance still falls short of the high-gain requirements necessary for applications such as hydrogen generation. The structure proposed in [28] improves upon the classic boost converter by incorporating voltage-lift techniques, yet the resulting gain does not sufficiently justify the increased number of components.

The converters presented in [29]–[32] achieve approximately double the voltage gain of the conventional boost topology; however, this increase does not constitute a significant performance enhancement. In contrast, the topology in [33] integrates two voltage multiplier cells within the classic boost converter structure. Although this design successfully isolates the common ground between the input source and the load, it is unable to generate sufficiently high output voltages from low input levels, limiting its applicability in hydrogen extraction systems. Reference [34] proposes an improved version of the classic buck-boost converter, achieving higher voltage gain than the base topology. Nonetheless, this design fails to address the inherent topological limitations of the original converter, and while its voltage gain surpasses that of traditional converters, it remains modest compared to other advanced topologies. In addition, in [49] and [50], two new quadratic step-up DC-DC converters with low input current ripple using switched capacitor techniques are suggested. However, these structures cannot offer ultra-high voltage gain.

This study proposes an improved cascaded boost topology featuring ultra-high voltage gain. The design incorporates an enhanced diode–capacitor voltage multiplier cell to achieve significant voltage lifting. Unlike conventional boost and cascaded boost converters, the proposed topology overcomes their main limitations, addressing issues related to voltage gain and component stress. The substantial voltage gain delivered by this converter makes it particularly well-suited for high-voltage applications, including dielectric test equipment and water electrolysis systems.

II. The Proposed Topology Function

The proposed topology is illustrated in Fig. 2(a). It is based on the integration of two diode–capacitor voltage multiplier cells-similar to those used in the improved topologies

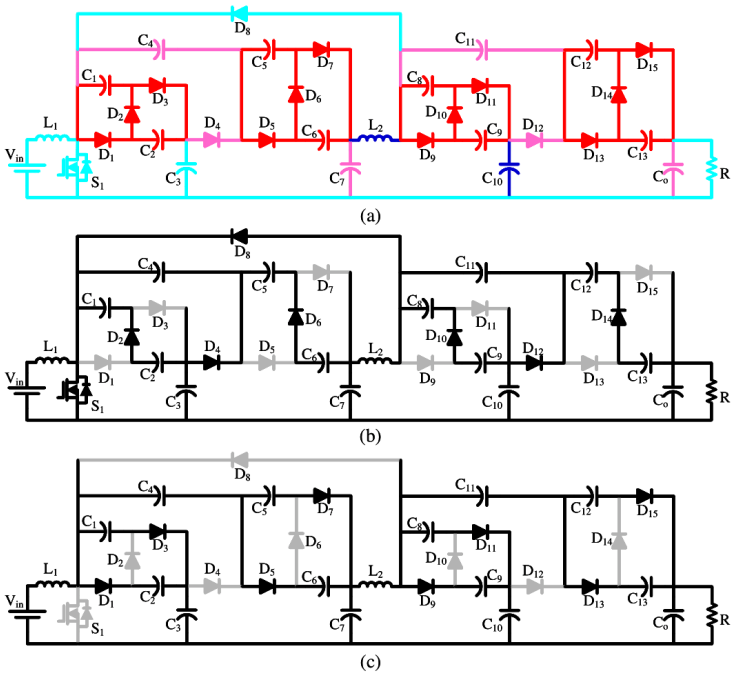


Fig.2. (a) Proposed converter, (b) The equivalent circuit of the first mode, (c) The equivalent circuit of the second mode.

shown in Figs. 1(b) and 1(c)-combined with an enhanced cascaded boost topology, as depicted in Fig. 1(e). Notably, the design utilizes only two inductors, matching the number found in classic converter topologies such as SEPIC, Ćuk, and Zeta. The input current in the proposed converter is continuous, with the input current ripple matching that of the inductor L_1. The switching device is positioned in the low-voltage section of the circuit, resulting in reduced voltage stress on the switch. The equivalent circuits corresponding to the first and second operating modes are illustrated in Figs. 1(b) and 1(c).

During the first operating mode, the voltage applied to the inductors is positive, causing them to magnetize. In this mode, capacitors C_3 and C_4, C_{10} and C_{11}, the series combination of C_1, C_2, and C_3, the series combination of C_8, C_9, and C_{10}, the series connection of C_4 through C_6 and C_7, and the series connection of C_{11} through C_{13} and C_o are all connected in parallel. In the second operating mode, the applied voltage to the inductors reverses polarity, causing them to demagnetize. During this interval, capacitors C_1 and C_2, C_5 and C_6, C_8 and C_9, C_{12} and C_{13}, the series combination of C_2 through C_5, and the series combination of C_9 through C_{12} with C_o are connected in parallel. According to the expressed concepts and the equivalent circuits, the inductors' voltage and capacitors' current in the steady state are as (1)-(16):

$$v_{L1} = DV_{in} + (1-D)(V_{in} + V_{C2} - V_{C3}) \quad (1)$$
$$v_{L2} = DV_{C7} + (1-D)(V_{c7} + V_{C9} - V_{C10}) \quad (2)$$
$$i_{C1} = Di_3 + (1-D)(-i_1) \quad (3)$$
$$i_{C2} = Di_3 + (1-D)(i_1 + i_6 - i_{L1}) \quad (4)$$
$$i_{C3} = D(-i_3 - i_4) + (1-D)(i_{L1} - i_6) \quad (5)$$
$$i_{C4} = D(i_4 + i_7) + (1-D)(-i_6) \quad (6)$$
$$i_{C5} = D(i_7) + (1-D)(-i_5) \quad (7)$$
$$i_{C6} = D(i_7) + (1-D)(i_5 - i_6) \quad (8)$$
$$i_{C7} = D(i_{10}) + (1-D)(-i_8) \quad (9)$$
$$i_{C8} = D(i_{10}) + (1-D)(-i_1) \quad (10)$$
$$i_{C9} = D(i_{10}) + (1-D)(i_8 + i_{14} - i_{12}) \quad (11)$$
$$i_{C10} = D(-i_{10} - i_{11}) + (1-D)(i_{L2} - i_{13}) \quad (12)$$
$$i_{C11} = D(i_{11} + i_{14}) + (1-D)(-i_{13}) \quad (13)$$
$$i_{C12} = D(i_{14}) + (1-D)(-i_{12}) \quad (14)$$
$$i_{C13} = D(i_{14}) + (1-D)(i_{12} - i_{13}) \quad (15)$$
$$i_{Co} = D(-i_{14} - I_o) + (1-D)(i_{13} - I_o) \quad (16)$$

In this context, currents i_1, i_3 through i_8, and i_{10} through i_{14} represent the inrush currents generated during the parallel connection of the capacitors. Based on the voltage-second balance principle, the average voltage across the inductors is zero. Similarly, according to the current-second balance, the average current flowing through the capacitors is zero. By applying these principles to equations (1)–(16), the average inductor currents, average capacitor voltages, and capacitor inrush currents are derived as shown in equations (17) and (28).

$$V_{C1} = V_{C2} = V_{C5} = V_{C6} = \frac{V_{in}}{1-D} \quad (17)$$
$$V_{C3} = V_{C4} = V_{C7} = \frac{4V_{in}}{1-D} \quad (18)$$
$$V_{C8} = V_{C9} = V_{C12} = V_{C13} = \frac{4V_{in}}{(1-D)^2} \quad (19)$$
$$V_{C10} = V_{C11} = \frac{8V_{in}}{(1-D)^2} \quad (20)$$
$$V_{Co} = \frac{8V_{in}}{(1-D)^2} \quad (21)$$
$$i_{L1} = \frac{16}{(1-D)^2} I_o \quad (22)$$
$$i_{L2} = \frac{4}{1-D} I_o \quad (23)$$

$$i_1 = i_5 = \frac{4}{(1-D)^2} I_o \quad (24)$$

$$i_3 = i_4 = i_7 = \frac{4}{D(1-D)} I_o \quad (25)$$

$$i_6 = \frac{8}{(1-D)^2} I_o \quad (26)$$

$$i_8 = i_{12} = i_{13} = \frac{I_o}{1-D} \quad (27)$$

$$i_{10} = i_{11} = i_{14} = \frac{I_o}{D} \quad (28)$$

The provided voltage gain in the cascaded boost converter is $\frac{1}{(1-D)^2}$. Comparing this voltage gain with the one provided in the proposed topology shows that the voltage gain in the proposed topology is 16 times that of the cascaded boost converter. Based on the derived voltage gain, Fig. 3 compares the performance of the proposed converter with the topologies presented in Fig. 1.

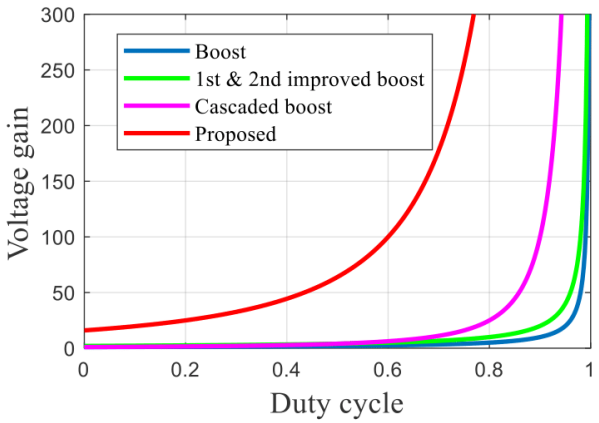


Fig. 3. Voltage gain comparison.

It is evident that at low duty cycles, the proposed topology delivers a higher voltage gain than the boost, improved boost, and cascaded boost converters operating at higher duty cycles. This comparison clearly demonstrates the superior performance of the proposed topology. The semiconductors' voltage/current stresses are as follows ((28)-(34)):

$$V_S = V_{D1-D7} = \frac{V_{in}}{1-D} \quad (28)$$

$$V_{D8} = \frac{(3+D)}{(1-D)^2} V_{in} \quad (29)$$

$$V_{D9} = V_{D10-D15} = \frac{4}{(1-D)^2} V_{in} \quad (30)$$

$$I_S = \frac{15+2D-D^2}{(1-D)^2} I_o \quad (31)$$

$$I_{D1-D7} = \frac{4}{1-D} I_o \quad (32)$$

$$I_{D8} = \frac{3+D}{1-D} I_o \quad (33)$$

$$I_{D9-D15} = I_o \quad (34)$$

To evaluate the operating conditions of the semiconductors, the voltage stresses are compared against the output voltage, while the current stresses are compared with the input current. The normalized values are illustrated in Fig. 4. As shown in Fig. 4(a), the voltage stresses on the semiconductors are significantly lower than the output voltage. Except for the switch, whose current stress approaches the input current level, the current stresses on all other components remain considerably below the input current. Therefore, all semiconductor devices operate within safe limits. The relatively low voltage stress on the semiconductors makes this converter especially suitable for low-voltage applications requiring high voltage gain, such as water electrolysis.

The simplified current ripple of the inductors and capacitors' voltage ripple are as (35) to (41).

$$\Delta i_{L1} = \frac{DV_{in}}{L_1 f_s}, \quad \Delta i_{L2} = \frac{4DV_{in}}{(1-D)L_2 f_s} \quad (35)$$

$$\Delta V_{C1} = \frac{4I_o}{(1-D)C_1 f_s}, \quad \Delta V_{C2} = \frac{4I_o}{(1-D)C_2 f_s} \quad (36)$$

$$\Delta V_{C3} = \frac{8I_o}{(1-D)C_3 f_s}, \quad \Delta V_{C4} = \frac{4I_o}{(1-D)C_4 f_s} \quad (37)$$

$$\Delta V_{C5} = \frac{4I_o}{(1-D)C_5 f_s}, \quad \Delta V_{C6} = \frac{4I_o}{(1-D)C_6 f_s} \quad (38)$$

$$\Delta V_{C7} = \frac{4(1+D)I_o}{(1-D)C_7 f_s}, \quad \Delta V_{C8} = \frac{I_o}{C_8 f_s} \quad (39)$$

$$\Delta V_{C9} = \frac{I_o}{C_9 f_s}, \quad \Delta V_{C10} = \frac{2I_o}{C_{10} f_s}, \quad \Delta V_{C11} = \frac{2I_o}{C_{11} f_s} \quad (40)$$

$$\Delta V_{C12} = \frac{I_o}{C_{12} f_s}, \quad \Delta V_{C13} = \frac{I_o}{C_{13} f_s}, \quad \Delta V_{Co} = \frac{(1+D)I_o}{C_o f_s} \quad (41)$$

Here, ΔV_{Ci} and f_s are the allowable voltage ripple of the capacitors and switching frequency, respectively.

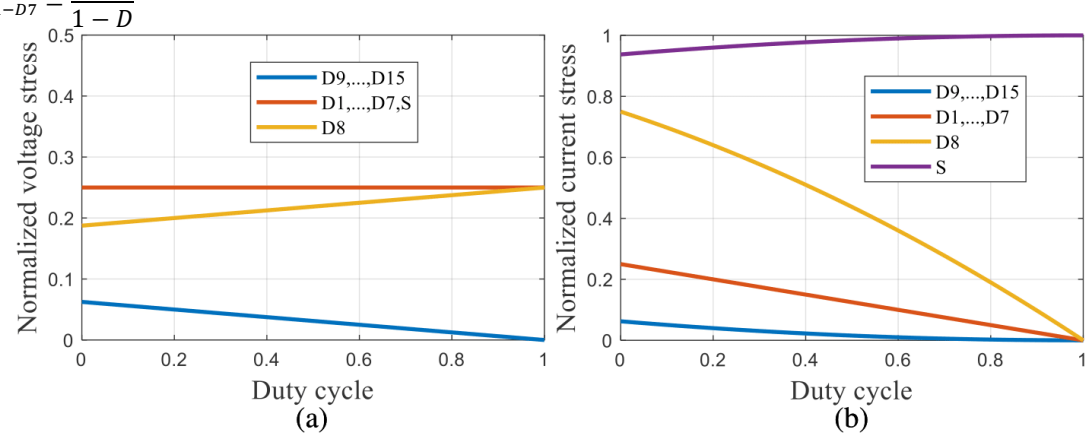


Fig. 4. Normalized voltage/current stresses of the semiconductors. (a) Normalized voltage stress, (b) Normalized current stress.

The operation of the converter in continuous conduction mode (CCM) depends on the inductors' values and their average currents. Specifically, the inductors' values influence the magnitude of the current ripple. To maintain CCM, the peak-to-peak current ripple of each inductor must be less than twice its average current. Based on this criterion, the minimum inductance required to sustain CCM is given by the following expression:

$$L_1 > \frac{D(1-D)^4 R}{512 f_s} \quad , L_2 > \frac{D(1-D)^2 R}{32 f_s} \tag{42}$$

Here, R denotes the output resistance. The average current through each inductor must exceed half of its corresponding current ripple to ensure continuous conduction mode (CCM). This average inductor current depends on both the duty cycle and the average output current. Fig. 5 illustrates the converter's operating regions, distinguishing between CCM and discontinuous conduction mode (DCM) based on output current and duty cycle. The equations used to generate this plot are provided in (43).

$$I_{OB} = \frac{V_{in}}{2L_2 f_s} D = \frac{V_o}{32 L_2 f_s} D(1-D)^2 \tag{43}$$

Which, I_{oB} is the boundary value of the output current between CCM and DCM. Notably, any operating point above the curves shown in Fig. 5 corresponds to continuous conduction mode (CCM), points below the curves indicate discontinuous conduction mode (DCM), and points lying on the curves represent the boundary between these two modes. Notably, the effect of the parasitic components of the circuit elements shows their effect in the higher percentages of the duty cycle. In other words, in the majority of the duty cycle percentage, the converter's function and parameters have the same behavior in both the model and non-ideal modes.

III. Non-Ideal Voltage Gain and Efficiency

The voltage gain derived in the previous section does not account for variations in component quality or changes in output power. By incorporating the resistances of the inductors (r_L), switch (r_S), and diodes (r_D), along with the load resistance (R), the non-ideal voltage gain is expressed as shown in equation (44).

$$\frac{V_o}{V_{in}} = \frac{16}{(1-D)^2} - \frac{r_L}{R}\frac{16^2}{(1-D)^6} - \frac{r_{SC}}{R}\frac{16^2 D}{(1-D)^6} - \frac{r_D}{R}\frac{16^2}{(1-D)^5} \tag{44}$$

Fig. 6 compares the ideal and non-ideal voltage gains. As shown, both curves closely align when the duty cycle is below 80%. Fig. 7 illustrates the voltage gain behavior under different output power levels and component variations. The results indicate that output power has the most significant impact on voltage gain. Additionally, the choice of inductor cores influences the equivalent series resistance, while different switches with varying dynamic resistances and diodes with distinct forward voltage drops are considered in this sensitivity analysis. Considering the conduction loss of inductors (P_L), switch (P_{SC}), and diodes (P_D) and ignoring the frequency loss of the components, the efficiency of the converter can be modelled as (45)-(48). Fig. 8 shows the efficiency sensitivity analysis considering different output power levels and circuit components. The results indicate that variations in output power have the greatest impact on efficiency. Changes in the type of inductor and switch exhibit approximately equal effects on efficiency.

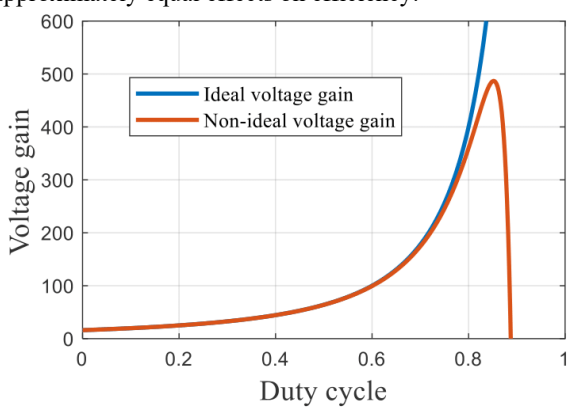


Fig. 6. Comparison of the ideal and non-ideal voltage gains.

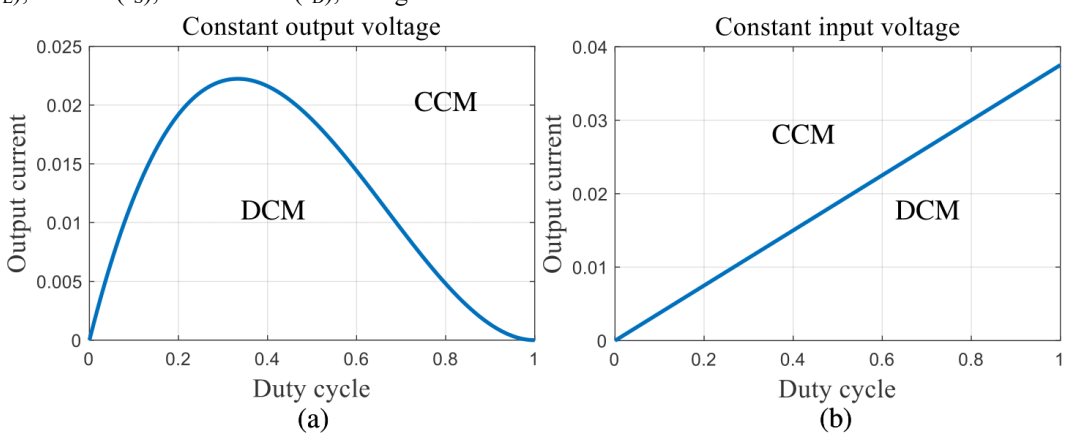


Fig. 5 The operational region of the converter in CCM and DCM while: (a) constant output voltage, (b) constant input voltage.

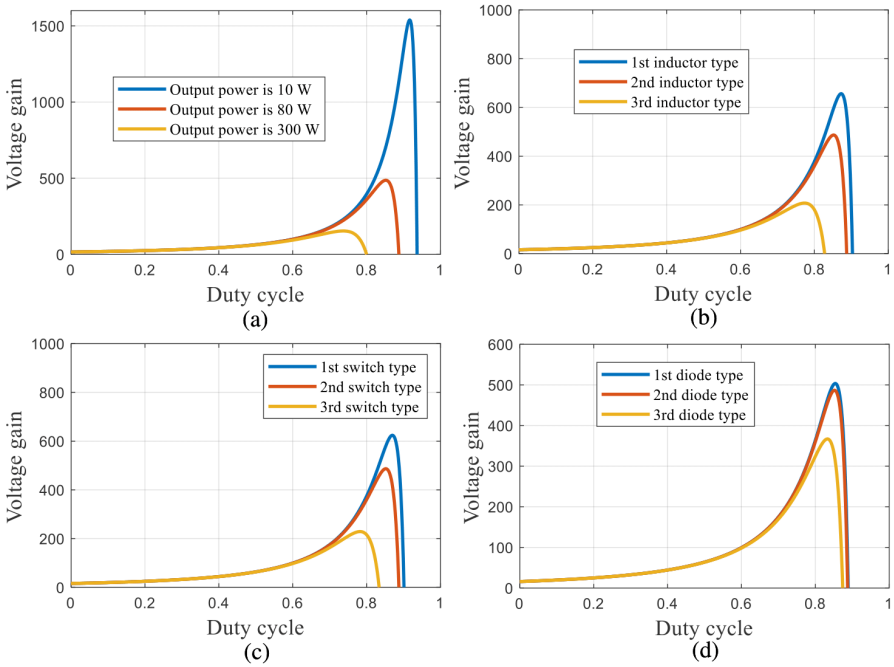


Fig. 7. Non-ideal voltage gain behavior while: (a) the output power is changing, (b) the inductor type is changing, (c) the switch type is changing, (d) the diode type is changing.

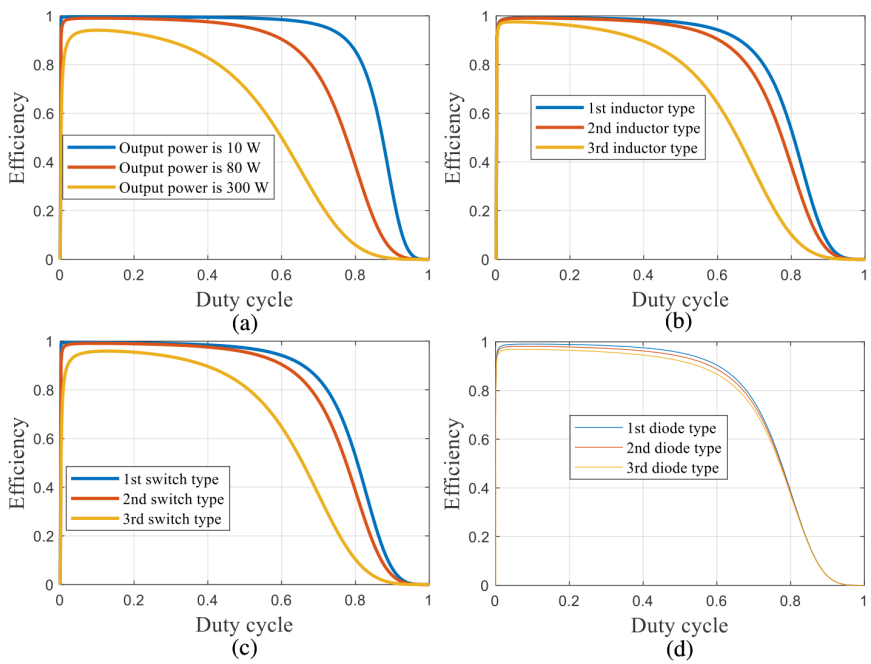


Fig. 8. Efficiency behavior while: (a) the output power is changing, (b) the inductor type is changing, (c) the switch type is changing, (d) the diode type is changing.

$$P_L = \frac{16(17-2D+D^2)}{(1-D)^4}\frac{r_L}{R}P_o \quad (45)$$

$$P_{SC} = \frac{(6+11D-D^2)}{D(1-D)^4}\frac{r_S}{R}P_o \quad (46)$$

$$P_D = \frac{(38-6D)}{1-D}V_{DF}I_o \quad (47)$$

$$\eta = \frac{P_o}{P_o + P_L + P_{SC} + P_D} \quad (48)$$

IV. Application of the Proposed Topology

The electrolysis of water is an electrochemical process that uses direct electric current (DC) to drive the non-spontaneous decomposition of water into its constituent elements, hydrogen (H_2) and oxygen (O_2). The Materials and Apparatus for this process are: Electrolytic Cell, Electrodes, Electrolyte, Power Supply, and Measurement Devices. Hydrogen is widely regarded as a clean energy source for the future. One common method of hydrogen production is water electrolysis, which can be performed at relatively low voltages. However, at low voltages, bubble formation around the electrodes tends to accumulate, reducing the efficiency of the electrolysis process. To mitigate this issue, applying a high pulsed voltage with an average value of approximately 10 V has been proposed, as it helps decrease bubble congestion around the electrodes. A high-gain DC-DC converter can be employed to supply the elevated voltage required for the DC link of the pulse power converter. Such a converter enables the generation of high voltages from low-voltage sources like batteries, power supplies, or photovoltaic panels. Fig. 9-10 provide the schematic illustration of the application of a high-gain DC-DC converter for water electrolysis in hydrogen extraction.

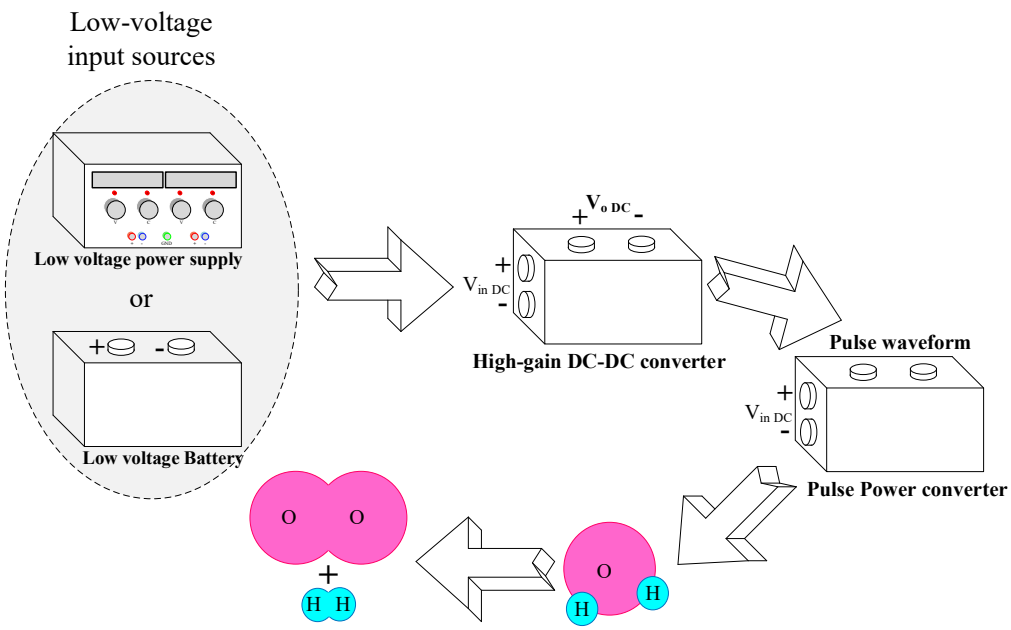


Fig.9. Symbolic presentation of using a high-gain DC-DC converter to electrolyze the water for hydrogen extraction.

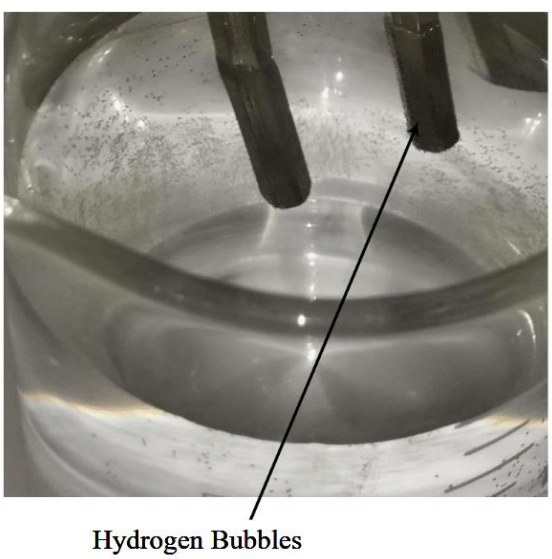


Fig. 10. The actual performance of the proposed converter in a water electrolysis setup.

V. Comparison Study

Fig. 11 compares the voltage gain and voltage gain density of various topologies. As shown, the proposed topology achieves a significantly higher voltage gain than those presented in [16]–[20]. Specifically, the voltage gain produced at low duty cycle percentages in the proposed converter exceeds that of the referenced topologies even at higher duty cycles. While the increased number of components in the proposed topology might be perceived as the reason for this improved gain, Fig. 11(b) addresses this by comparing voltage gain density as “voltage gain per total number of active and passive components (inductors, capacitors, diodes, and switches)”. In this analysis, the voltage gain of each topology is normalized by its respective component count to provide a fair comparison. As illustrated in the figure, the proposed topology exhibits a higher voltage gain density compared to the others, demonstrating its superior design for achieving elevated voltage gain.

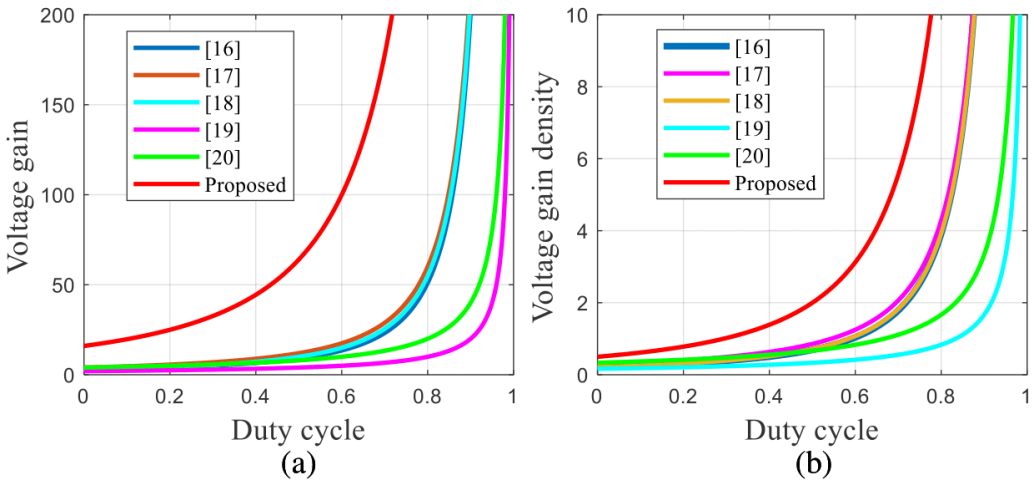


Fig. 11. Comparison results of the proposed topology and recently suggested topologies. (a) Voltage gain (b) voltage gain density.

VI. Experimental Results

The prototype converter is designed by specifying the voltage and current characteristics of the circuit components and selecting appropriate values for the capacitors and inductors. Table I summarizes key parameters, including input voltage, switching frequency, inductor current ripple, capacitor voltage ripple, output current, and duty cycle. Based on these values and the equations presented in Section 2, Table II details the average capacitor voltages, average inductor currents, and voltage/current stresses on the semiconductor devices. Additionally, Table II presents the minimum required inductance and capacitance values derived from the current and voltage ripple specifications discussed in Section 2. Based on the components' expressed voltage/current characteristics, the component types used in the prototype are listed in Table III. Fig. 12 depicts the constructed prototype of the proposed converter based on the outlined design concepts. The first step to reduce the EMI is to provide the continuity of the input current. This factor was provided in the proposed topology. The second effective factor in EMI is the hot loops. Hot loops are current paths, which their current value changes from zero to a non-zero value. The most important hot-loop in DC-DC converters is the current path of the input current to switch. In the proposed topology, the switch is used at the first part of the cascaded parts, and the switch position is as close as possible to the input source terminal. In order to reduce the EMC, the continuity of the input current is provided. Additionally, the inductors were shielded to reduce the DM noises. Experimental results are presented in Fig. 13-19, illustrating the current waveforms of the inductors, voltage waveforms of the capacitors, and voltage and current waveforms of the semiconductor devices.

A comparison between these measured waveforms and the corresponding values reported in Table II demonstrates strong agreement. The minor discrepancies observed are attributed to losses and voltage drops caused by parasitic elements.

Fig. 20 shows the efficiency characteristics under different conditions: Fig. 20(a) displays efficiency versus output current at a constant output voltage, while Fig. 20(b) shows efficiency versus output voltage at a constant output power. The results confirm that the converter maintains acceptable efficiency levels.

According to the presented curves in Fig. 20, the extracted efficiency at P_o=80 W, and V_o=1200 V, is about 94%. Notably, this high efficiency is due to the high value of the voltages and low value of the currents, which keeps the losses in a low value and negligible range. In other words, changing the operating point can change the extracted efficiency. The reported efficiency in the recently suggested converters is shown in Table IV. It is worth noting that for output voltages exceeding 1200 V (as demonstrated in the experiments), two such converters can be connected in series, as illustrated in Fig. 21. In this configuration, the input voltages must be isolated from one another, and the switch of the second converter requires a high-side drive.

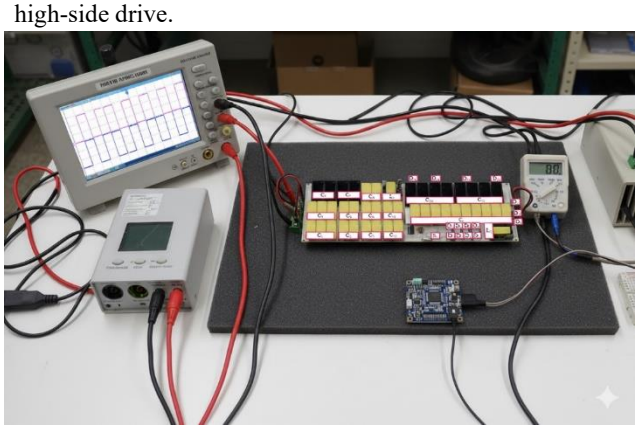


Fig. 12. A photo of the prototype of the proposed converter.

TABLE I. DESIGN CONSIDERATIONS.

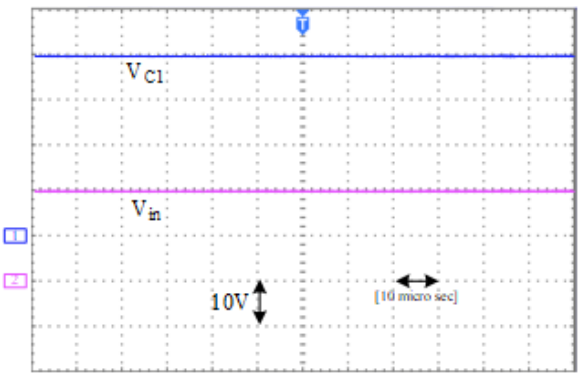
V_{in}	I_o	f_s	D	Δi_L	Δv_c
20V	62.5mA	50kHz	0.5	30%	5%

TABLE II. PREDICTED VALUES BY THE THEORETICAL RELATIONS.

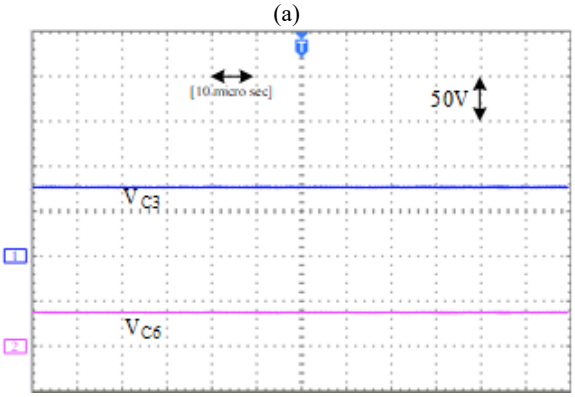
parameter	value	parameter	value	parameter	value
$V_{C1,2,5,6}$	40 V	$V_{C3,4}$	80 V	V_{C7}	160 V
$V_{C8,9,12,13}$	320 V	$V_{C10,C11}$	640 V	V_o	1280 V
I_{L1}	4 A	I_{L2}	0.5 A	$V_{S,D1,\ldots,D7}$	40 V
$V_{D9,\ldots,D15}$	320 V	V_{D8}	280 V	$I_{D1,\ldots,D7}$	0.5 A
$I_{D9,\ldots,D15}$	62.5 mA	I_{S1}	3.93 A	I_{D8}	0.43 A
L_1	166 μH	L_2	10 mH	$C_{1,\ldots,6}$	5 μF
$C_{8,\ldots,13}$	78 nF	C_o	30 nF		

TABLE III. COMPONENTS TYPE.

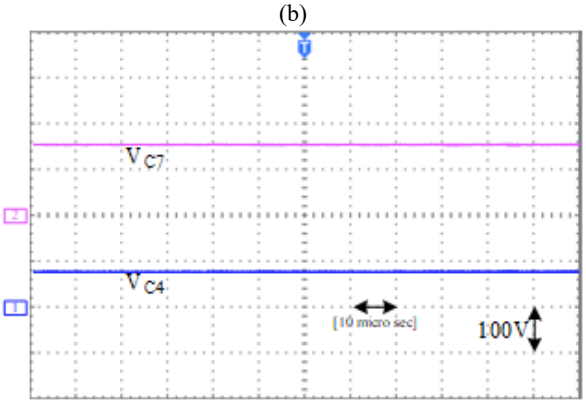
Inductor	Capacitor	diode	Switch
EC type	MKT	DTV56F	IRF540



(a)

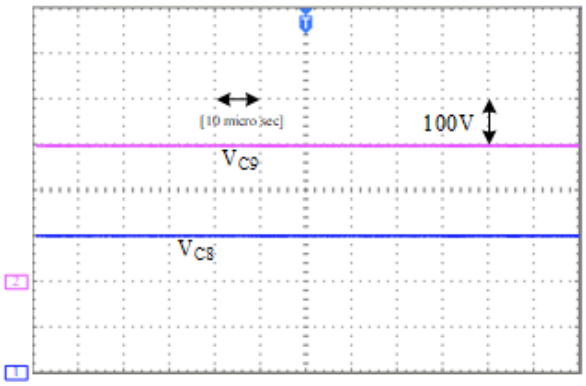


(b)

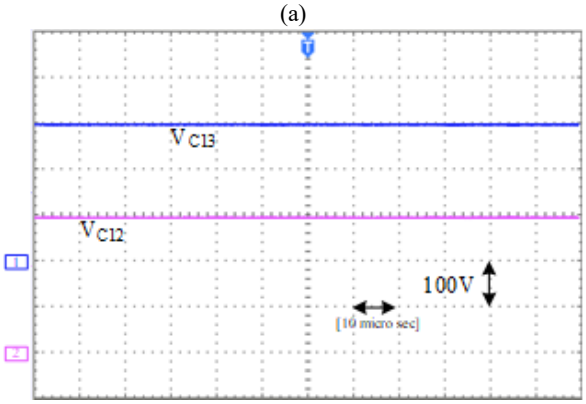


(c)

Fig. 13. Experimental results. (a)V_{C1} and V_{in} (b) V_{C3}, V_{C6}, and (c) V_{C4}, V_{C7}.



(a)



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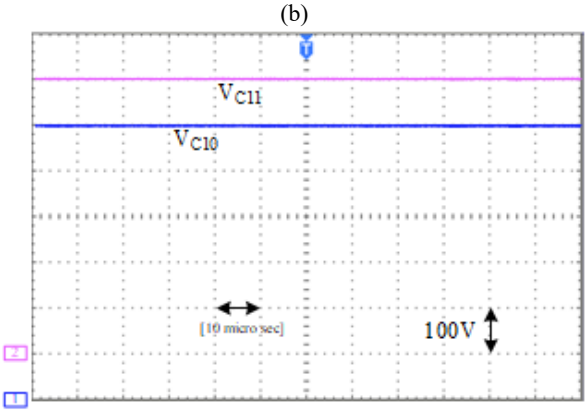

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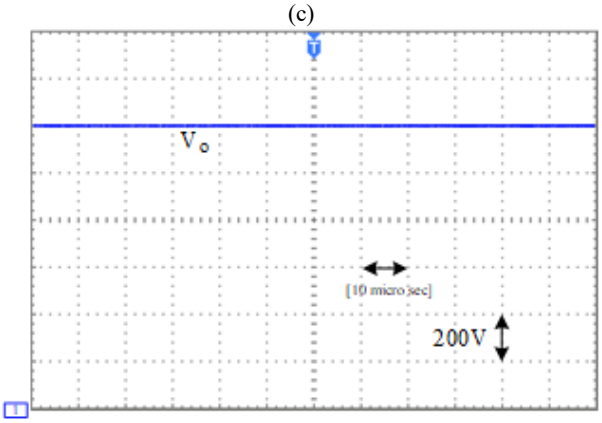


(d)

Fig. 14. Experimental results. (a) V_{C9}, V_{C8} , (b) V_{C12}, V_{C13}, (c) V_{C11}, V_{C10}, and (d) V_{Co}.

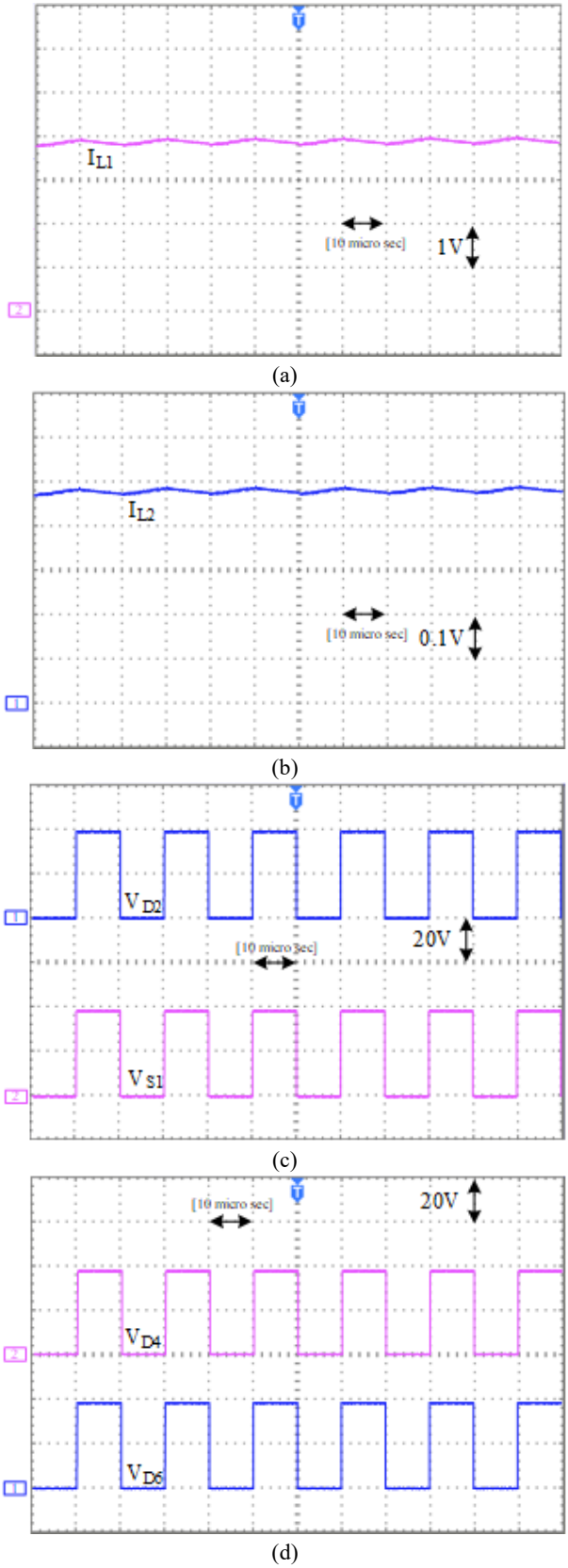


Fig. 15. Experimental results of the proposed converter. (a) I_{L1}, (b) I_{L2}, (c) V_{S1}, V_{D2}, and (d) V_{D4}, V_{D6}.

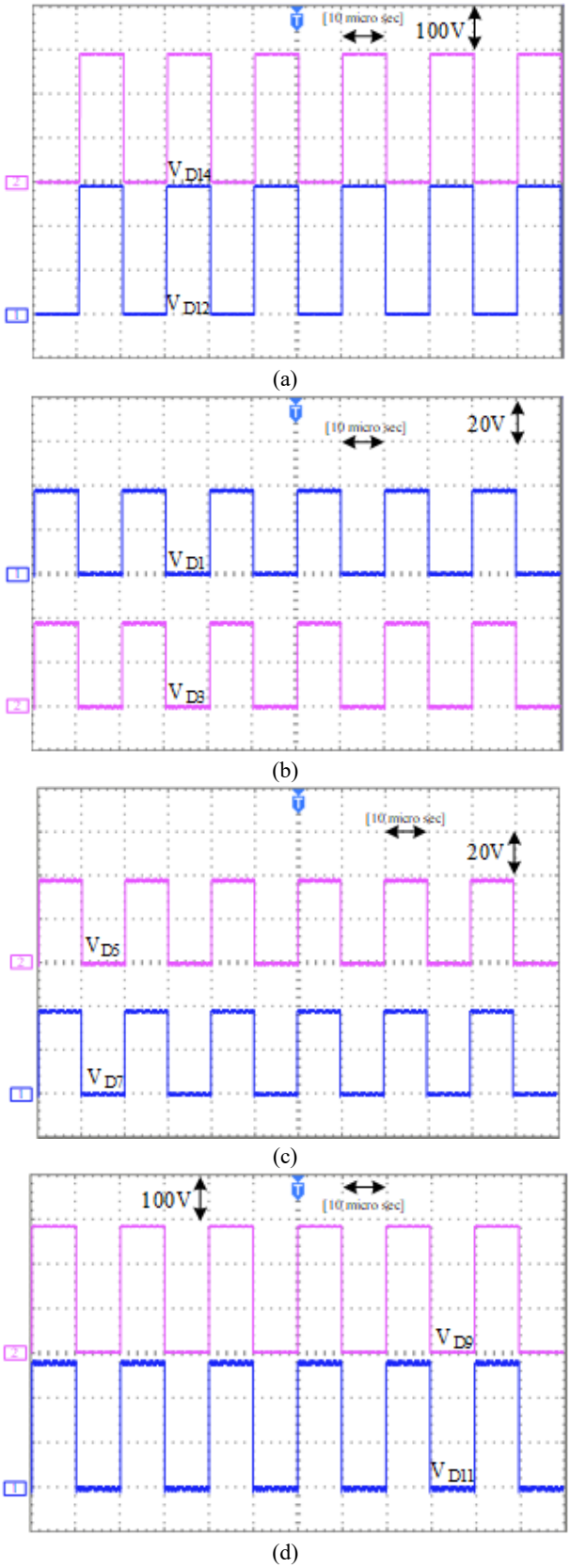
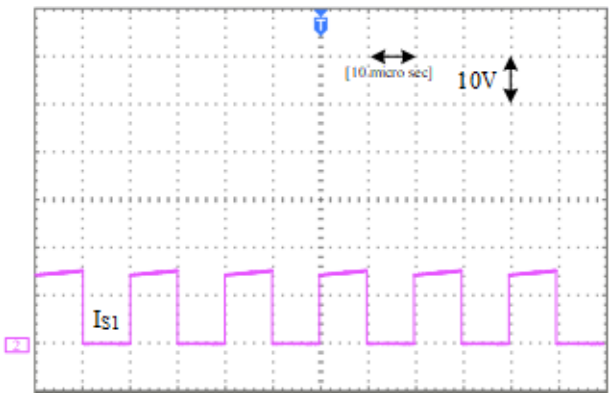
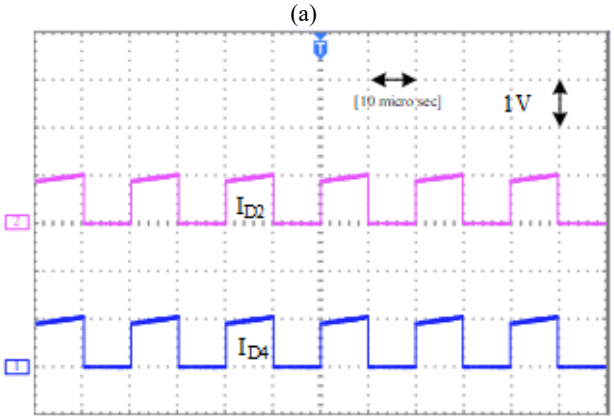


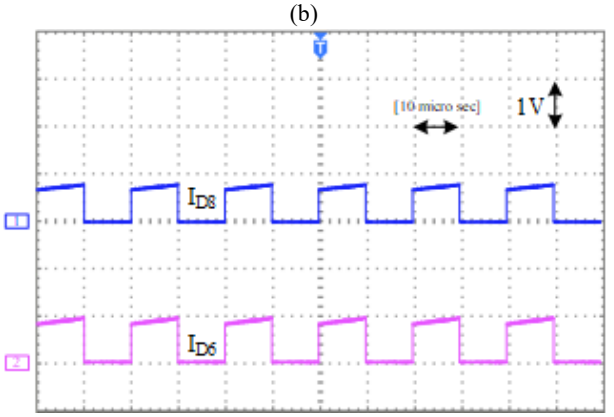
Fig. 16. Experimental results. (a) V_{D12}, V_{D14}, (b) V_{D1}, V_{D3}, (c) V_{D5}, V_{D7}, and (d) V_{D9}, V_{D11}.



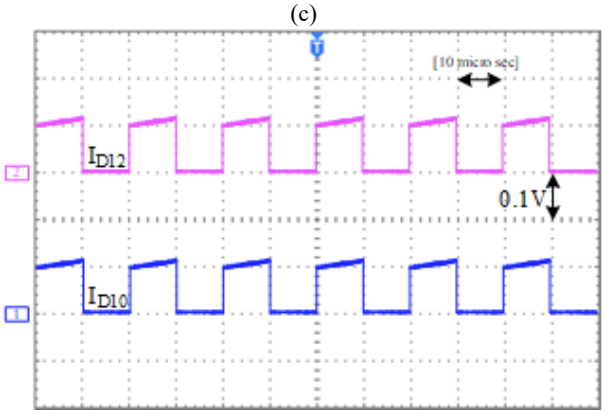
(a)



(b)

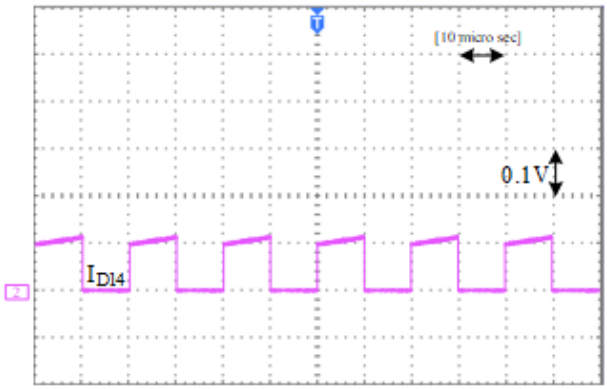


(c)

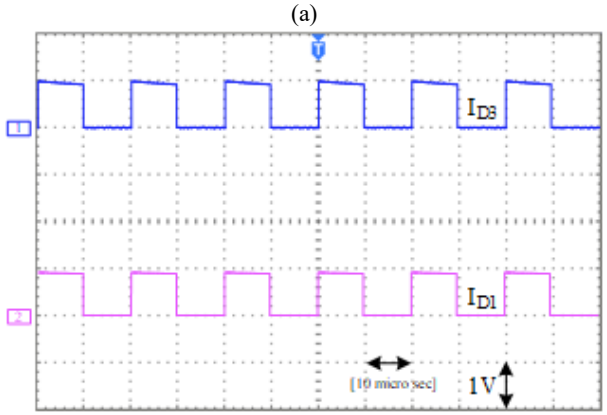


(d)

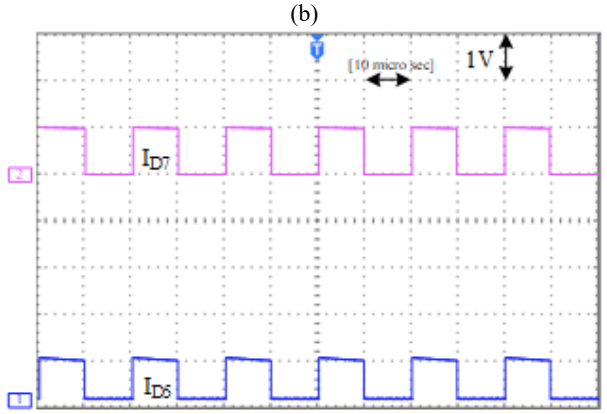
Fig. 17. Experimental results of the proposed converter. (a) I_{S1}, (b) I_{D2}, I_{D4}, (c) I_{D6}, I_{D8} and (d) I_{D12}, I_{D10}.



(a)



(b)



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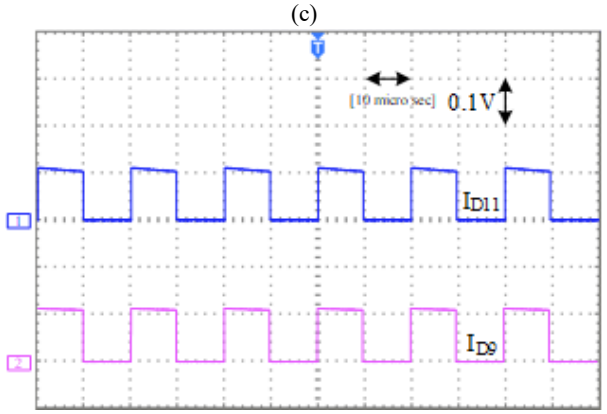

(d)

Fig. 18. Experimental results of the proposed converter. (a) I_{D14}, (b) I_{D1}, I_{D3}, (c) I_{D5}, I_{D7}, and (d) I_{D9}, I_{D11}.

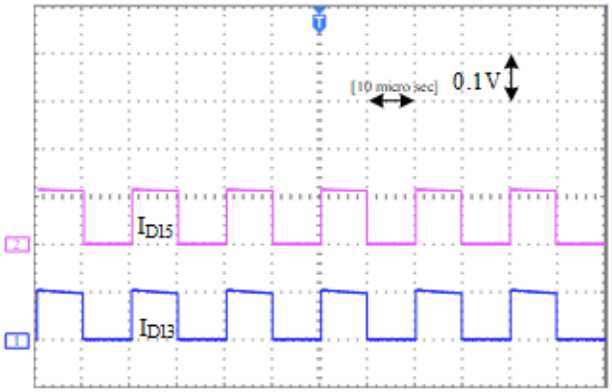

Fig. 19. Experimental results of I_{D13}, I_{D15}.

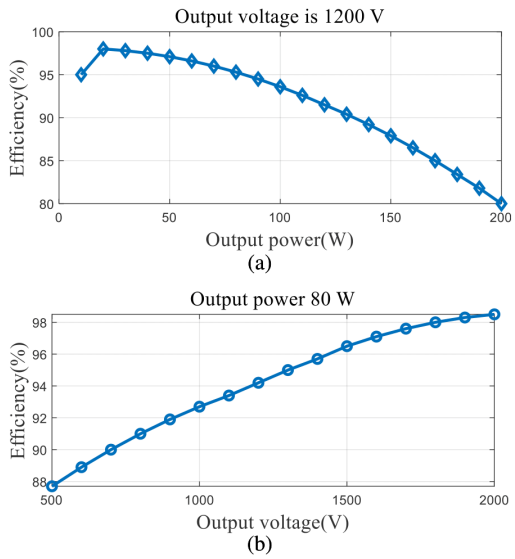

Fig. 20. The measured efficiency of the proposed converter.

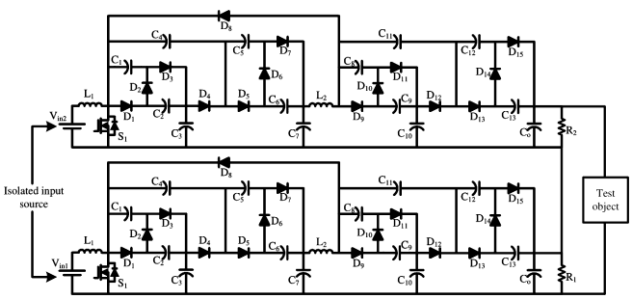

Fig.21. Two series connection of such converters.

TABLE IV. COMPONENTS OF THE MEASURED EFFICIENCY OF THE CONVERTERS.

Converter	Measured efficiency	Rated Power
[16]	93%	60W
[17]	90%	100 W
[18]	92.96%	150 W
[19]	93%	70 W
[20]	94.6%	250 W
[21]	90%	100 W
[22]	93.8%	100 W
[23]	93.1%	50 W
[24]	94.7%	100 W
[25]	97%	100 W
[27]	90%	100 W
[29]	94%	100 W
[30]	95.5%	100 W
[35]	93%	100 W
[36]	95.8%	100 W
[37]	93%	100 W
[38]	91%	100 W
[42]	97%	100 W
[43]	94.2%	100 W
[44]	96.5%	100 W
[45]	90%	100 W
[56]	91%	100 W
[47]	90.5%	100 W
[48]	95.1%	100 W

VII. Conclusion

This study presented an improved cascaded boost topology featuring a novel quadratic voltage-lift effect, achieving significantly higher voltage gains at lower duty cycles. In addition to the high voltage gain, the voltage stress on the semiconductors remains well below the output voltage, and their current stress is considerably less than the input current, enhancing device reliability. Experimental results demonstrated the converter's ability to boost a 20 V input to 1200 V output at a 50% duty cycle, validating the theoretical analysis. Furthermore, the compact prototype design enables series connection of multiple converters to reach output voltages up to approximately 6 kV, making it suitable for high-voltage applications such as dielectric testing.

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Mohammad Reza Shaker Ardakani received the B.S. degree in electronic engineering from Azad Islamic University, Yazd Branch, Iran, in 2000, and M.S. degree from Azad Islamic University, Abarkouh Branch Iran, in 2015. He is now a Ph.D candidate in the Islamic Azad University, Najafabad branch Najafabad, Iran.

Sara Hasanpour was born in Iran, in 1979. She received the B.S. degree in electronic engineering from Azad Islamic University, Lahijan Branch, Iran, in 2002, the M.S. degree from the Isfahan University of Technology, Isfahan, Iran, in 2005, and the Ph.D. degree in power electronics engineering from University of Guilan, Rasht, Iran, in 2019. She is currently assistant professor at Azad Islamic University, Ramsar Branch, Ramsar, Iran. Dr. Hasanpour is a frequent reviewer of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, IEEE TRANSACTIONS ON POWER ELECTRONICS and IET POWER ELECTRONICS. Moreover, she is an Associate Editor of IEEE JOURNAL OF EMERGING AND SELECTED TOPICS IN INDUSTRIAL ELECTRONICS.

Majid Moazzami was born in 1982. He received the B.Sc. and M.Sc. degree in Electrical Engineering from Azad Najafabad University (Isfahan-Najafabad/Iran) in 2004 and 2007 respectively. He received PHD degree in Electrical Engineering department of Isfahan University. Since 2008, He is with the Department of Electrical Engineering of Islamic Azad University-Najafabad branch in Iran. He is associated professor of IAUN and IEEE Senior Member. His main areas of research interest are Power system dynamics, stability and control, electricity markets, renewable energy & micro grids, and smart grids.

Fariborz Haghighatdar Fesharaki was born in Isfahan, Iran, in 1981. He received the B.Sc. degree in electrical engineering from Islamic Azad University of Najaf Abad, Iran, in 2005 and the M.Sc. (Honors) and Ph.D. degrees, both in electrical engineering from University of Isfahan, Iran, in 2008 and 2014, respectively. His research interests include power system quality assessment and computational methods in power system monitoring and operation.

Mahnaz Hashemi was born in Isfahan, Iran. She received her B.Sc., M.Sc., and Ph.D. degrees in Electrical Engineering from the Department of Electrical and Computer Engineering, Isfahan University of Technology, Isfahan, Iran, in 2007, 2010 and 2015. Since 2013, she has been with the Department of Electrical Engineering at Najafabad Branch, Islamic Azad University, Najafabad, Iran. She is currently an associate professor at Electrical Engineering Department of Najafabad Branch, Islamic Azad University. She has published more than 50 journal and conference papers. Her current research interests include adaptive control, nonlinear systems, fractional order systems and fault tolerant control.