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An Improved Method for Capacitor Voltage Balancing Control and Capacitance Monitoring in Modular Multilevel Converter

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ABSTRACT

The modular multilevel converter (MMC) has emerged as a leading topology for high-voltage and high-power applications, owing to its scalable modular structure, elimination of bulky output filters, and independence from multiple DC sources. Despite these advantages, the large number of capacitors in the MMC introduces substantial reliability challenges, particularly with respect to maintaining accurate voltage balance. Conventional balancing techniques typically rely on numerous voltage sensors, thereby increasing system cost and complexity while compromising reliability. This paper presents an improved capacitor voltage balancing strategy that significantly enhances the reliability of MMCs. The proposed approach employs a single voltage sensor shared between two half-bridge submodules (HB-SMs), thereby simplifying the sensing architecture and ensuring accurate capacitor voltage estimation with minimal hardware. Moreover, the strategic placement of the sensor enables an integrated capacitance monitoring scheme capable of assessing capacitor health in real time, further improving system robustness. The validity and effectiveness of the proposed method are demonstrated through comprehensive simulation and experimental results under a wide range of operating conditions.

I. Introduction

Recently, multi-level converters (MCs) have attracted the interest of many researchers [1], [2]. Compared to two-level converters, MCs have great advantages, such as producing high-quality AC voltages, low THD, reducing the voltage or current of semiconductors and switching frequency [3], [4]. Among the types of MCs, the modular multilevel converter (MMC) is recognized as one of the most important emerging developments for high voltage direct current (HVDC) systems [5], [6]. In industrial applications, half-bridge sub-modules are generally employed in MMC topology [7]. Thus, a large number of flying capacitors have been employed in the topology of MMCs based on HB-SM, and regulating the voltage balance of these capacitors is one of the main challenges of using MMC [8]. In order to balance the voltage of the capacitors, instantaneous information about the voltage of the capacitors is required, which necessitates the use of a large number of voltage sensors, where the number of voltage sensors is the same as HB-SMs [9], [10]. Using this number of voltage sensors affects the converter's expense, reliability, and complexity, mainly when a converter with a high number of levels is considered [11].

In recent years, numerous studies have concentrated on reducing the number of sensors in Modular Multilevel Converters (MMC). Table 1 presents a comparison of methods aimed at sensor reduction in MMC.

In references [12], [13], [14], techniques have been introduced to decrease the number of current sensors. However, these methods do not address the reduction of voltage sensors. Moreover, reducing current sensors causes the malfunction of open-circuit fault detection and circulation current-control systems in the MMC.

In [15], the concept of group measurement (GM) for capacitor voltage is introduced, necessitating a minimum of two voltage sensors in each arm. However, an advanced voltage balancing algorithm must be applied to the system, where activating and deactivating numerous SMs instantaneously may cause instability. Additionally, in the

proposed technique, the update of capacitor voltage depends on the time when only one SM is active in the group, thereby compromising the accuracy of predicting capacitor voltage.

TABLE I Comparison of capacitor capacitance monitoring methods

Reference	Method	Online /Offline	N. Voltage sensor	Low switching frequency	High switching frequency	Calculation burden	error
[22]	RLS algorithm and second harmonic current injection	Online	N	NO	Yes	Low	1.3%>
[23]	KFA algorithm	Online	N	NO	Yes	High	*
[24]	RSUBM	Online	N	NO	Yes	Low	3%>
[25]	Using the MMC DC-Side Start-Up feature	Offline	N	*	*	*	1%>
[26]	Using the discharge curve of submodule capacitors and parallel resistors	Online	N	NO	Yes	Low	2%>
Proposed method	Ratio of estimated to measured voltage Increase	Online	N/2	Yes	Yes	Low	1% >

TABLE II Comparison of sensor reduction methods

Reference	Number of voltage sensors in the arm	Number of Current Sensors in the Arm	Calculation burden	Reliability	Capacitance monitoring	Voltage ripple of capacitors
[12-14]	N	0	Medium	Low	No	<5%
[15]	At least two	1	Medium	Medium	No	10%
[16]	0	1	Very high	Low	No	<4%
[17]	Number of groups	1	Very high	High	Yes	<10%
[18]	1	0	Very high	Low	No	<6%
[19]	N/2	1	Medium	High	NO	<5%
Proposed method	N/2	1	Low	High	Yes	<5%

The adaptive linear neuron

(ADALINE) algorithm is used in [16] to track SM voltage dynamics. Despite the promising results, this method requires accurate arm inductor voltage measurement. In [17], a self-updating capacitor voltage method based on group measurement of SM output voltage is presented, which has raised the accuracy of capacitor voltage estimation. However, the estimation method is very complex, making it difficult to use in practical applications. In [18], an improved method for estimating capacitor voltage using Kirchhoff equations with only arm voltage sensors and output current sensors is presented. The system's reliability is decreased when the arm current sensors are removed, and updating the

voltage of the capacitors depends on the forced activation algorithm. In [19], an optimized algorithm was introduced that reduces the number of voltage sensors by grouping submodules and simultaneously enables capacitor voltage balancing and fast open-circuit fault detection, validated through both simulations and experiments. The forced activation approach leads to system instability when using a high number of HB-SMs in actual applications. According to the above contents and the results of Table 1, the solutions to reduce the sensor have three major drawbacks:

a. the computational burden grows exponentially as the number of submodules rises, which makes the application of these methods challenging in MMCs with a large number of SMs;

b. the majority of these methods require high-voltage sensors or sensors with high galvanic isolation voltage;

c. most methods reduce the reliability of converter performance. Due to these three constraints, approaches for

reducing the voltage of sensors in industrial applications have received little attention.

Furthermore, the MMC topology's large number of capacitors has harmed the converter's reliability, since capacitors with a 30% failure rate are among the most common sources of faults in power electronic systems [19]. In power electronics applications, three types of capacitors are often used [20]: electrolytic capacitors (E), metalized polypropylene film capacitors (MPPF), and multilayer ceramic capacitors (MLC). These capacitors are vulnerable due to internal or external variables, such as the aging effect, chemical reactions, and excessive threshold voltages. Capacitor failures decrease the MMC's availability and cause severe explosions and even loss of life [21]. Therefore, capacitance monitoring is essential to detect faulty capacitors as a solution. Table 2 compares the capacitor capacitance monitoring methods. The recursive least-squares (RLS) approach for capacitance estimate utilizing capacitor voltage, capacitor current, and submodule switching mode information is presented in reference [22]. In this approach, an AC current is injected into the circulating current, which increases the voltage ripple of the capacitors. As a result, the control process will be complicated, and the performance of the MMC will be affected. In [23], the Kalman-filter algorithm and instantaneous information of capacitor current and voltage are used for capacitance monitoring, but this algorithm complicates the capacitance estimation. Reference [24] describes a capacitance monitoring technique based on the reference submodule, in which the capacitance is estimated based on the capacitor voltage relationship between the reference submodule and other submodules. The most significant drawbacks of this method are the vast number of voltage sensors required and the requirement of a complicated sorting algorithm. An off-line capacitance monitoring method is presented in [25], which uses the relation between phase current and SM voltage at the stage of MMC startup to estimate the capacitance. However, this method has no online capacitance monitoring and only works at the stage of MMC startup. In [26], a method based on the characteristic of discharging capacitors is presented, that in each capacitance monitoring, a target sub-module is bypassed from each arm, to discharge the capacitors up to 0.368 times the rated capacitor voltage. Despite the realization of online monitoring in this method, the voltage stress in other capacitors increases, and the recharging process of the bypassed sub-modules causes the instability of the system. As a result, the reliability of MMC decreases. In [27], a capacitance health monitoring scheme for MMCs was introduced that minimizes the number of voltage sensors while maintaining a low computational burden. This approach enables

accurate and efficient assessment of capacitor conditions, and its effectiveness has been validated through both simulation and experimental studies.

This paper introduces an improved approach for regulating capacitor voltage balance, employing the GM

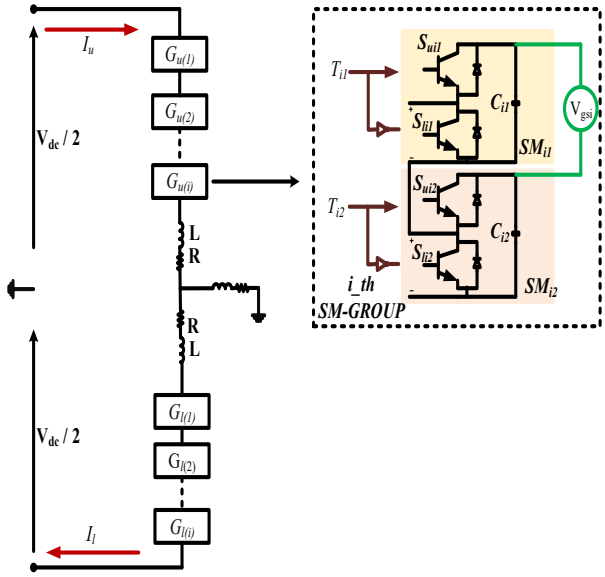

Fig. 1. Single-phase MMC arrangement based on GM

methodology for capacitor voltage control. The proposed method employs the capacitor voltage and current equation to estimate capacitor voltage, ensuring heightened accuracy in estimation without incurring additional computational burden. Furthermore, leveraging the specific arrangement of voltage sensors, a novel Capacitance Monitoring Method is presented to enhance the reliability of the MMC. This monitoring method utilizes the ratio between estimated and measured increases in capacitor voltage. Within each operational cycle, an indicator meticulously assesses the health status of capacitors, issuing a fault warning promptly upon detecting any anomalies in capacitor performance. These advancements contribute not only to the precision of capacitor voltage control in MMC but also exemplify the commitment to enhancing the reliability and robustness of high-power applications.

II. Configuration of GM

The schematic representation of the single-phase MMC configuration, featuring two arms (upper and lower arms), is illustrated in Fig.1. Each arm is constructed through the series connection of i (i=1, 2, ...N/2) groups, arm resistance (R), and arm inductor (L). Within each group, a voltage sensor (Vgsi) and two half-bridge submodules (SMij (j=1, 2)) are employed. The group voltage sensor is strategically positioned between the two positive poles of the submodule capacitors. The half-bridge submodule structure integrates two switches (Suij, Slij) and a capacitor (Cij). The switching state of the Half-Bridge Submodule (HB-SM), delineated in Table 3, is regulated by the switching function (Tij). When Tij=1, the capacitor is placed in the circuit; if Iarm>0, the capacitor's voltage (V_{cij}) increases; otherwise, the capacitor

discharges. Also, if $T_{ij}=0$, the capacitor will be bypassed and the voltage of the capacitor will remain unchanged.

TABLE III HB-SM switching state

T_{ij}	Upper (S_{uij}) switch	Lower (S_{lij}) switch	I_{arm}	V_{cij}
1	ON	OFF	>0	Charge
			<0	Discharge
0	OFF	ON	>0	Unchanged
			<0	

III. Proposed estimation method of capacitor voltage

In typical MMC systems, each HB-SM has an individual sensor connected in parallel to the SM capacitor. To maintain the capacitors' voltage balance, these sensors must continuously accumulate information regarding the capacitors' voltage. Therefore, the data exchange rate between the processor and the power system increases significantly. In this paper, the number of sensors in the GM-based configuration is reduced by half, and it is necessary to estimate the capacitor voltage to maintain the capacitor voltage balance. In this way, a simple estimation method is proposed in two steps, which are described below.

Step 1: Voltage measurement of capacitors

Fig. 2 shows the current path of the arm in step 1 in the SMs of the group. According to Fig. 2, in step 1 of voltage estimation of capacitors, according to the switching state (T_{ij}), certain states occur in which the value measured by the group voltage sensor is equal to the voltage of each capacitor. These special states are as follows:

T_{i2} = 0: As shown in Fig 2 (a), in this case, the voltage sensor (V_{gsi}) is parallel to C_{i1}, and the capacitor voltage is measured directly by the group sensor:

$$V_{gsi}(t) = V_{Ci1}(t) \quad (1)$$

T_{i1} = 0 and, T_{i2} = 0: In this case, according to Fig. 2 (b), the voltage value measured by the group sensor is equal to the voltage difference of the group capacitors, so:

$$V_{gsi}(t) = V_{Ci1}(t) - V_{Ci2}(t) \Rightarrow V_{Ci2}(t) = V_{Ci1}(t) - V_{gsi}(t) \quad (2)$$

Step 2: Voltage estimation of capacitors

According to the above analysis, in certain switching conditions, the voltage value of the capacitors can be directly measured by the group voltage sensor. On the other hand, capacitor voltage balancing needs real-time voltage data. In this way, it is necessary to estimate the voltage of capacitors in various switching conditions. As a result, when the group voltage sensor cannot be used to directly measure the capacitor voltage, the following equation can be used to estimate the capacitor voltage:

$$\hat{V}_{Cij}(t) = V_{Cmij} + \frac{1}{C_{ij}}\int_{t_0}^{t} i_{C_{ij}}(t)\ dt \quad (t = t_0 + k_{ij}T_s < t_1) \quad (3)$$

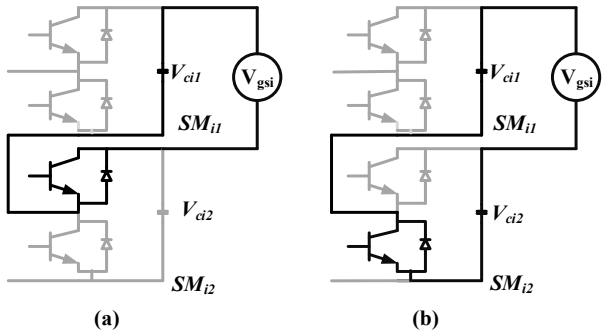

Fig. 2. Block diagram for capacitor voltage measurement in the step 1 of the estimation method, (a) T_{i2} = 0, (b) T_{i1} = 0 and, T_{i2} = 0

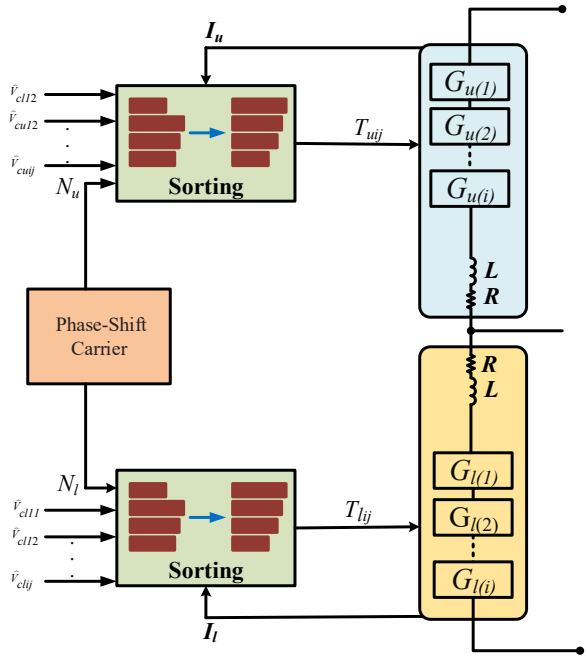

Fig. 3. Block diagram of MMC operation with the proposed estimation method

where $\hat{V}_{Cij}(t)$ is the estimated capacitor voltage, C_{ij} is the capacitor's nominal capacitance, i_{Cij} is the current flowing through the capacitor, T_s is the sampling time, V_{Cmij} is the capacitor's most recent measured voltage, k_{ij} is the number of sampling times in the estimation step, and t_0 and t_1 are the beginning and stop of the estimation mode, respectively. Consequently, the voltage of the capacitors of each group can be obtained using (1) - (3). A block diagram of the converter's operation while using the proposed technique, which uses PSC-PWM modulation, is given in Fig. 3. Also, in Table 4, the pseudo-code of the method of estimating and sorting the voltage of capacitors is presented. The number of inserted

HB-SMs (N_u, N_l) in the upper and lower arms is determined by comparing the reference signals with triangular carriers

TABLE IV Algorithm of the process of estimating and sorting the voltage of capacitors

1.	Start
2.	Check switching status
3.	if $T_{i2} == 0$ then
	$V_{gsi}(t) = V_{Ci1}(t)$
	else if $T_{i1} == 0$ and $T_{i2} == 0$ then
	$V_{Ci2}(t) = V_{Ci1}(t) - \underline{V_{gsi}}(t)$
	else
	$\hat{V}_{Cij}(t) = V_{Cmij} + \frac{1}{C_{ij}}\int_{t_0}^{t} i_{C_{ij}}(t)\ dt\ (t = t_0 + k_{ij}T_s < t_1)$
4.	Calculate Nu and determine T_{ij}
5.	
6.	Nu = Calculate Nu ()
	if $Nu == 0$ then
	$T_{ij}(t) = T_{il}(t\text{-}1)$
	else if $Nu > 0$ and $I_{arm} > 0$ then
	Choose the SMs with the highest voltage
	else if $Nu > 0$ and $I_{arm} < 0$ then
	Choose the SMs with the lowest voltage
7.	End of process

and using the PSC-PWM algorithm. Then, the best HB-SMs are chosen for insertion using the sorting algorithm to preserve the capacitors' voltage balance, and the switching state of the SMs of each arm (T_{uij}, T_{lij}) is produced. The predicted voltage of the capacitors and the current of the arms serve as the sorting algorithm's input variables. In accordance with the arm current direction's sign, if the arm current direction is positive, the SM with the lowest capacitor voltage will be selected, and if the arm current direction is negative, the SM with the highest capacitor voltage will be selected.

IV. The proposed capacitance monitoring method

The enormous number of capacitors in the MMC architecture decreases the system's reliability. According to the proposed configuration of the voltage sensors, an extreme decreasing the nominal value of the capacitance will result in a variance in the estimated voltage values of the capacitors. Therefore, capacitance continuous monitoring will be advantageous to raise the proposed configuration's reliability and improve its performance. Table 3 shows that if $I_{arm} > 0$, the capacitors' voltage rises. As a result, the proposed method uses the ratio of estimated to the measured capacitor voltage in $I_{arm} > 0$. According to section 3, the voltage of the capacitors can be measured directly by the group sensor in step (1). Thus, if $V_{m1(ij)}$ (the first capacitor voltage measured in the interval $I_{arm} > 0$) is the voltage measured at t_0 and $V_{m2(ij)}$ (the second voltage measured in the interval $I_{arm} > 0$) is the voltage measured at t_1, the measured voltage increase will be (For a better understanding, the pseudo-code of the proposed capacitance monitoring method is given in Table 5. Also, the block diagram of the capacitance monitoring process is shown in Fig. 4.):

$$\Delta V_{e1(ij)} = \frac{1}{C_{(ij)}}\int_{t_0}^{t_1} I_{arm}\, dt \tag{4}$$

where $\Delta V_{e1(ij)}$ is the estimated voltage increase value.
The voltage increase rate between the estimated capacitor voltage and the measured capacitor voltage can be determined using (4) and (5) as follows:

$$\frac{\Delta V_{e1(ij)}}{V_{m2(ij)} - V_{m1(ij)}} = \frac{C_{act(ij)}}{C_{(ij)}} = \frac{\Delta V_{e1(ij)}}{\Delta V_{m1(ij)}} \tag{5}$$

So, during the interval (t_0 - t_1), the actual value of the capacitance can be obtained through (6). Nevertheless, since the capacitance changes are not instantaneous, using (6) in small intervals, such as (t_0 - t_1) will increase the burden of calculations. Additionally, SMs switching frequency is higher than the arm's current frequency. Therefore, assuming that during the interval $I_{arm} > 0$ in an SM, there is k number of intervals like (t_0 - t_1) which causes the capacitor voltage to increase. Therefore, the equations (4) - (6) can be calculated in separate intervals, and applied as follows:

$$\Delta V_{m1(ij)} = V_{m2(ij)} - V_{m1(ij)} = \frac{1}{C_{act(ij)}}\int_{t_0}^{t_1} I_{arm}\, dt \tag{6}$$

In (4), $\Delta V_{m1(ij)}$ is the value of the voltage increase measured during the interval ($t_0 - t_1$), and $C_{act(ij)}$ is the actual value of the capacitance. The value of estimated voltage increases in the interval ($t_0 - t_1$) will be equal to:

$$\frac{\Delta V_{e1(ij)}}{\Delta V_{m1(ij)}} = \frac{\Delta V_{e1(ij)}}{V_{m2(ij)} - V_{m1(ij)}} = \frac{C_{act(ij)}}{C_{ij}}$$

$$\frac{\Delta V_{e2(ij)}}{\Delta V_{m2(ij)}} = \frac{\Delta V_{e2(ij)}}{V_{m3(ij)} - V_{m2(ij)}} = \frac{C_{act(ij)}}{C_{ij}} \tag{7}$$

$$\frac{\Delta V_{ek(ij)}}{\Delta V_{mk(ij)}} = \frac{\Delta V_{ek(ij)}}{V_{mk(ij)} - V_{mk-1(ij)}} = \frac{C_{act(ij)}}{C_{ij}}$$

It can be deduced from (7) that only the first and last voltage measured during the interval $I_{arm} > 0$ is required to calculate the actual capacitance. Therefore, (7) can be rewritten as follows:

$$\frac{\sum_{z=1}^{k} \Delta V_{ek(ij)}}{V_{mk(ij)} - V_{m1(ij)}} = \frac{C_{act(ij)}}{C_{(ij)}} \tag{8}$$

In (8), $V_{mk(ij)}$ and $V_{m1(ij)}$ are the maximum and minimum measured voltages during the interval $I_{arm} > 0$, respectively. As a result, the ratio of the sum of estimated to measured

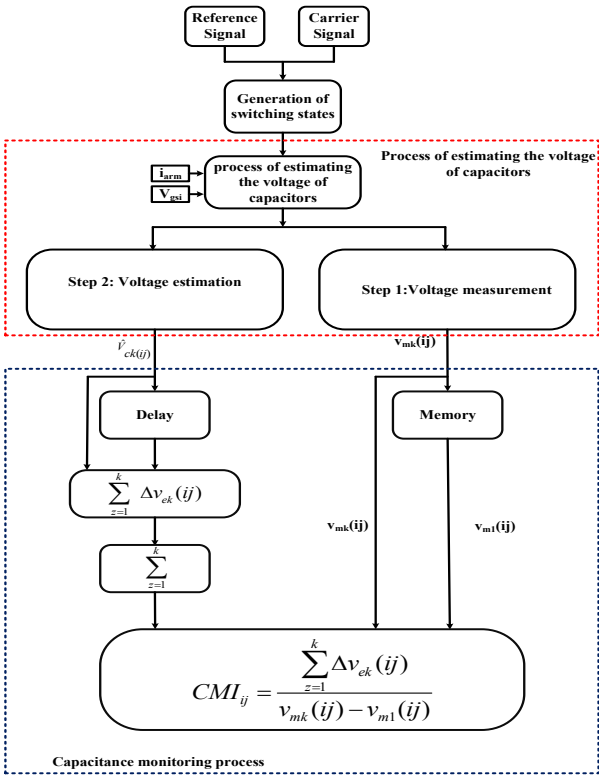

Fig. 4. Block diagram of the capacitance monitoring process

TABLE V CMI range for the failure of capacitor technology

Capacitor technology	CMI range for capacitor failure
E	CMI < 0.8
MPPF	CMI < 0.95
MLC	CMI < 0.9

voltage can be used to create a capacitance monitoring indicator (*CMI*):

$$\mathrm{CMI}_{(ij)} = \frac{\sum_{z=1}^{k} \Delta V_{ek(ij)}}{V_{mk(ij)} - V_{m1(ij)}} \quad (9)$$

The suggested indicator shows the ratio of the actual to nominal capacitance that is less than one. Depending on the type of capacitor technology of the MMC configuration, using the *CMI* index, there are different ranges for indicating failure in a capacitor, as shown in Table 6.

V. Simulation validation

A discrete-time validation of the proposed method has been performed using MATLAB/Simulink. The performance of the MMC operations with the proposed method was analyzed in different scenarios, such as steady state, transient state, switching frequency change, and abrupt input voltage change. Additionally, the proposed voltage estimation method was compared to the method introduced in [17],

TABLE VI Algorithm of the process of capacitance monitoring method

1. Begin Procedure

2. Monitor Capacitance

3. Calculate voltage increase during the interval (t_0 - t_k)

$\Delta V_m = V_{mk(ij)} - V_{m1(ij)}$

4. Calculate estimated voltage increase

$\Delta V_{e1(ij)}$

5. Calculate capacitance monitoring indicator (CMI)

$$CMI_{(ij)} = \frac{\sum_{z=1}^{k} \Delta V_{ek(ij)}}{V_{mk(ij)} - V_{m1(ij)}}$$

6. Use *CMI* to assess capacitance health

If CMI_{ij} > (*CMI* range for capacitor failure) then

Print ("Capacitance is within a healthy range.")

else

Print ("Fault Detection.")

end If

7. End Procedure

TABLE VII Critical parameters of the simulation and experimental evaluation

Items		Simulation values	Experimental values
DC terminal voltage (Vdc)		10 kV	120 V
Number of HB-SMs (N)		10	4
Nominal capacitance (C_{nam})		3200 µF	2200 µF
Nominal voltage of capacitors (V_{nam})		1 kV	30 V
Rated Modulation index (M_a)		0.87	0.9
Switching frequency (F_{sw})		1 kHz	500 Hz
Fundamental frequency (F_b)		50 HZ	50 Hz
Sampling time (Ts)		5e-5 s	2e-4 s
Arm inductance (L)		5 mH	5 mH
Output load	Resistance (Ro)	30 Ω	30 Ω
	Inductor (Lo)	17 mH	17 mH

which will be referred to as the reference method from now on. Table 7 presents the parameters employed in the simulation.

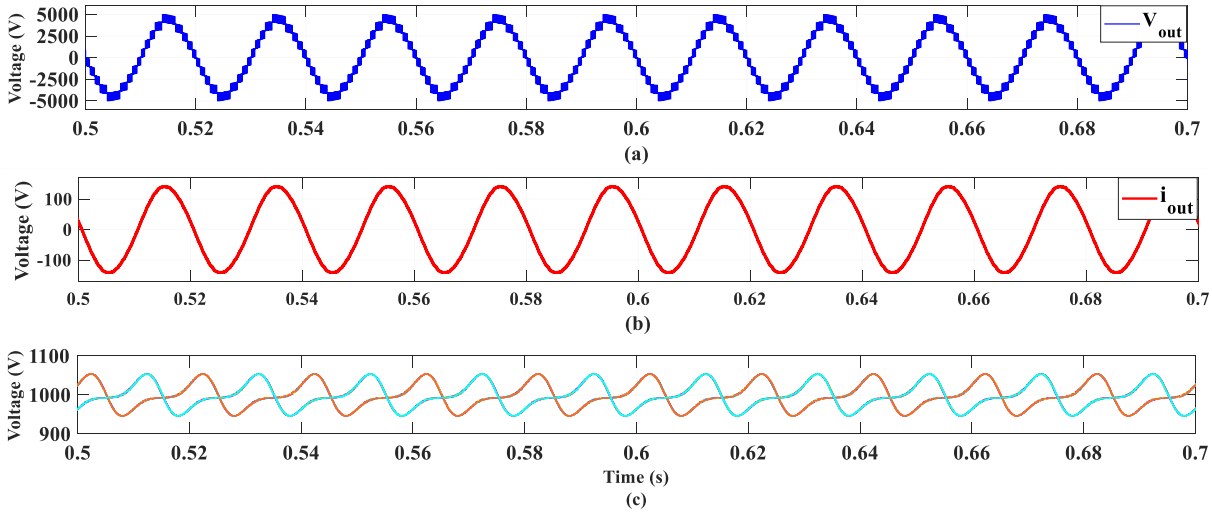

Fig. 5. Simulation results in steady-state conditions (proposed estimation method) (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage

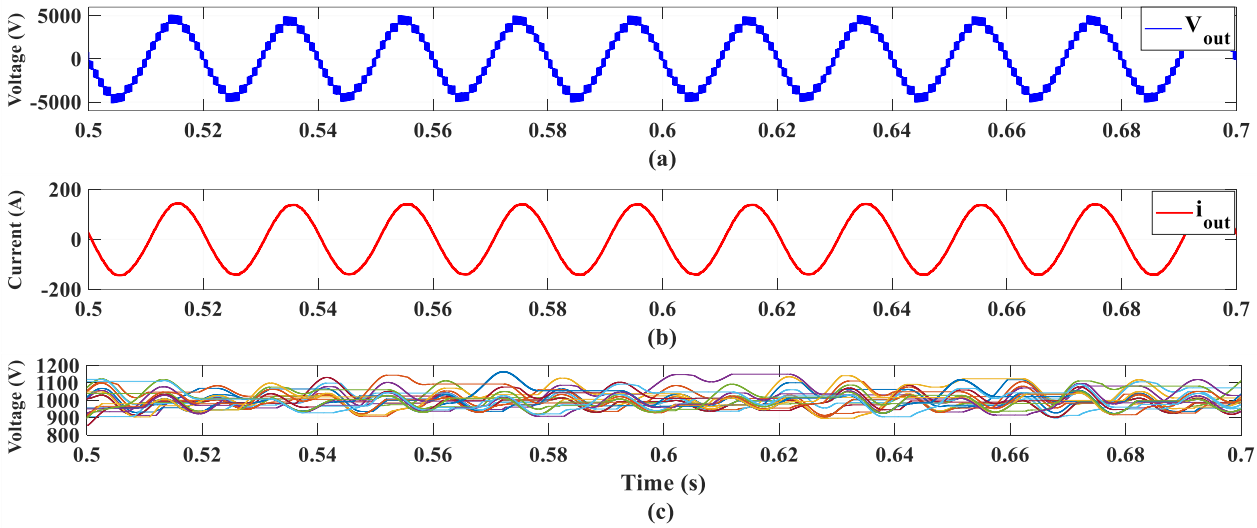

Fig. 6. Simulation results in steady-state conditions (Reference method) (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage

A. Performance of steady-state conditions

In this section, the results of simulating the proposed estimation method are evaluated in steady-state conditions with RL constant load. First, the proposed estimated method is used to evaluate the capacitors' voltage balance method, and then the same test is run using the reference method. Fig. 5 and Fig. 6 displays the simulation results for this scenario using the proposed and reference method. The voltage and output current have the same performance as the proposed estimate (Fig 5 (a) and Fig 5 (b) and the reference method (Fig 6 (a) and Fig 6 (b)). However, the proposed estimating approach outperforms the reference method in terms of the capacitors' voltage balance. In the reference method, the ripple voltage of the capacitors is $10\%V_{nam}$, while the ripple voltage of capacitors with the proposed method is $5\%V_{nam}$. This demonstrates the proposed estimation method's superiority to the reference method. Fig. 7 and Fig. 8 displays the estimated and measured capacitor voltages for HB-SM_{u11} and HB-SM_{u12}. Comparing the suggested technique to the reference method, it can be seen that the estimated values with the proposed method closely match the measured values. As a result, under steady-state operating conditions, the proposed method performs better than the reference method.

B. Performance of transient conditions

Fig. 9 – 12 show an evaluation of the performance of the proposed estimation method and reference method under transient situations, such as changing the DC side voltage and switching frequency. The conditions under which the DC side voltage is decreased by 25% V_{dc} in t = 0.6 s are shown in Fig. 9 and Fig. 10. The range of output current and voltage

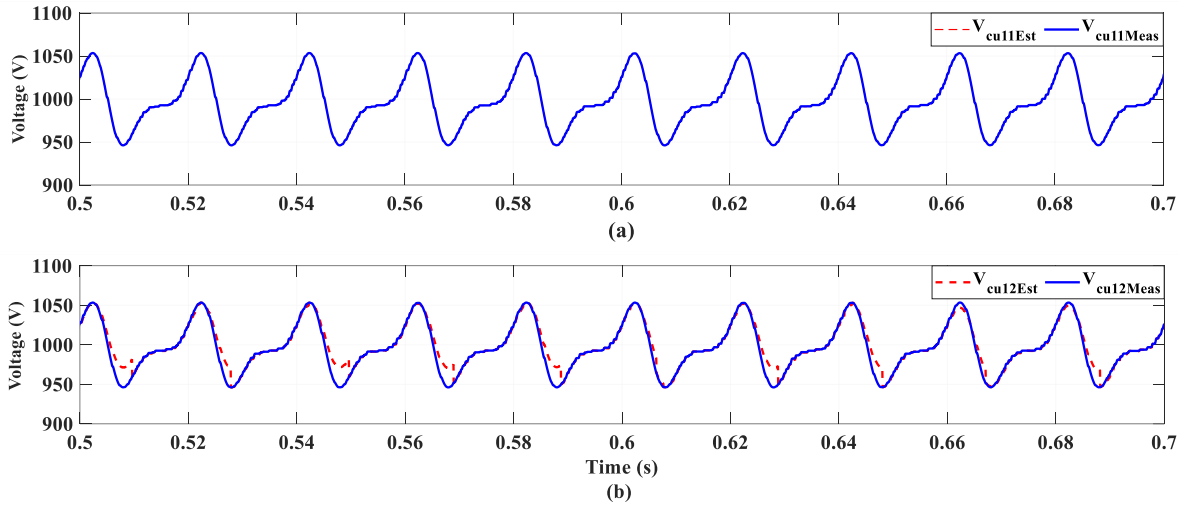

Fig. 7. Estimated and measured capacitor voltage (proposed estimation method) (a) HB-SM_{u11} capacitor voltage, (b) HB-SM_{u12} capacitor voltage

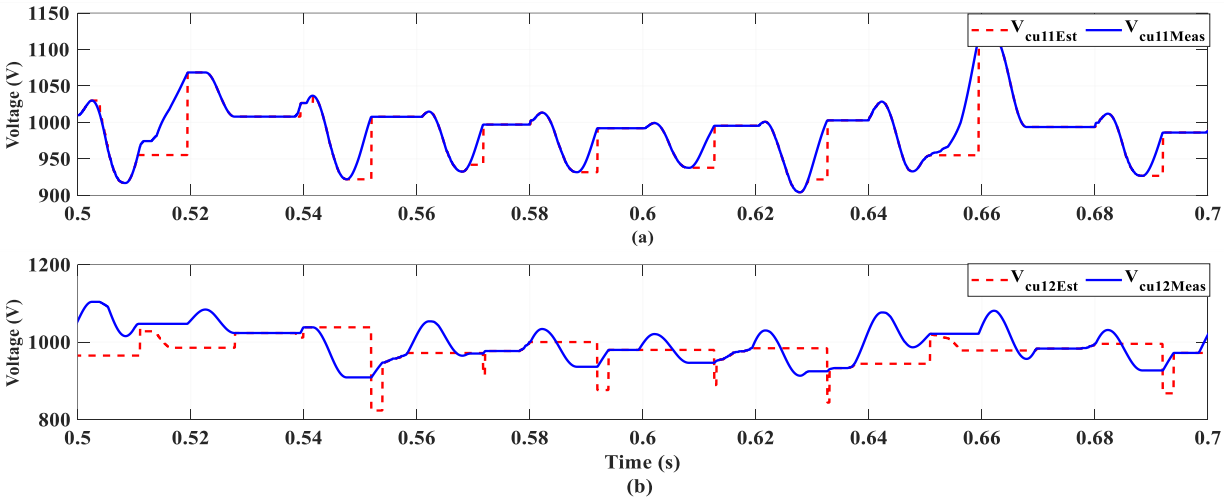

Fig. 8. Estimated and measured capacitor voltage (Reference method) (a) HB-SM_{u11} capacitor voltage, (b) HB-SM_{u12} capacitor voltage

have been decreased in both methods by reducing the DC side voltage, and the capacitors' voltages are now balanced at 7500V. However, the proposed method has a short transient period because the crossing of the transient conditions for the proposed and reference estimating procedures is 0.1s and 0.15s, respectively. In another scenario, the switching frequency is decreased from 1000Hz to 150Hz at t = 0.6s; Fig. 11 and Fig.12 compares the performance of the proposed method and the reference method. As expected, the disturbance in the current and voltage on the AC side has increased in both techniques after decreasing the switching frequency. However, the voltage ripple of the capacitors in the reference method has reached 20% V_{nam}, whereas it is only 6% V_{nam} in the proposed method. As a result, when compared to the reference method, the proposed voltage estimation method performs better at low switching frequencies.

C. *Performance of the proposed monitoring method*

The simulation results of the proposed monitoring approach when C_{u11} and C_{u12} are adjusted in their nominal value are shown in Fig. 13 and Fig. 14. Increasing the measured and estimated voltage for C_{u11} and C_{u12} are shown in Fig. 13 (a),

Fig. 13 (b), Fig. 14 (a) and Fig. 14 (b). The first and last measured voltages during each positive arm current cycle are denoted as $V_{m1}(ij)$ and $V_{mk}(ij)$, respectively. Fig. 13 (c) displays the capacitance monitoring indicator for C_{u11}, which is $CMI_{u11} = 1 \pm 0.2\%$ according to equation (13). Also, the capacitance monitoring indicator for C_{u12} is shown in Fig.13 (c), which for this capacitor is $CMI_{u12} = 1 \pm 0.4\%$. In another case, the capacitances of C_{u11} and C_{u12} are reduced by 25% and 20%, respectively, compared to the nominal capacitance, i.e., 2400 µF and 2560 µF, respectively. The simulation results of the proposed monitoring approach are shown in

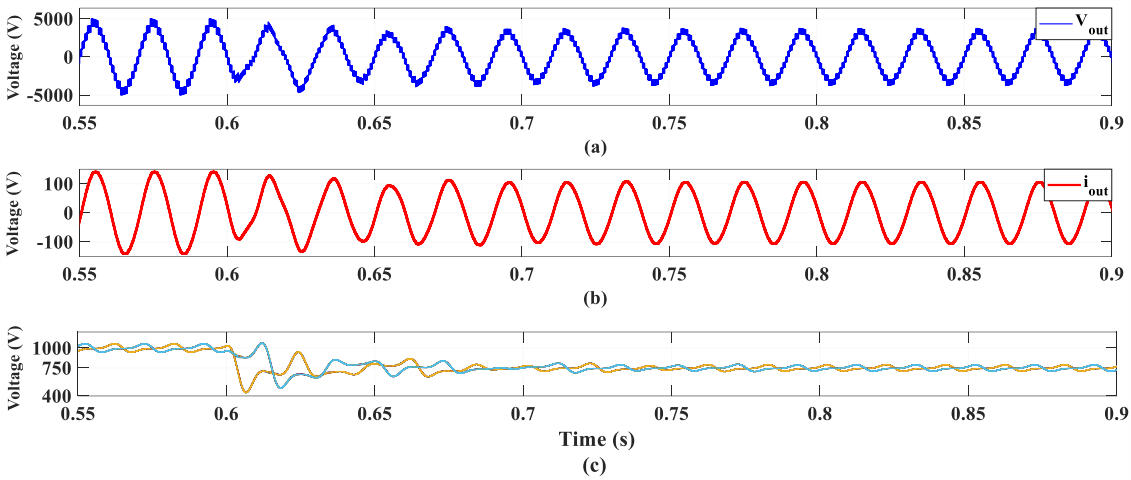

Fig. 9. Simulation results in DC side voltage changing conditions (proposed estimation method) (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage

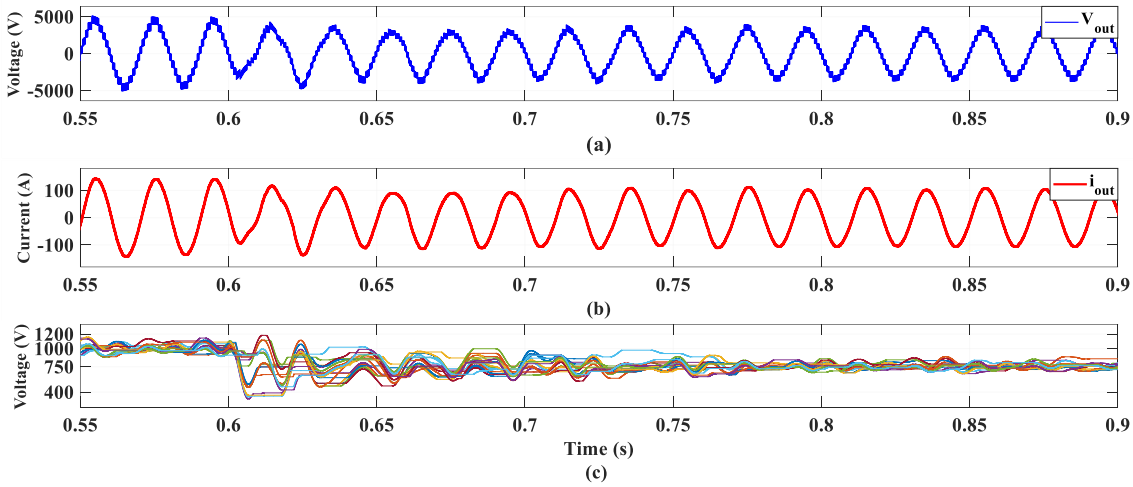

Fig. 10. Simulation results in DC side voltage changing conditions (Reference method) (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage

Fig. 15. The measured capacitor voltage increase is shown in Fig. 15 (a), and it is greater due to the lower actual capacitance of the voltage ripple of C_{u11}. Fig. 15 (b) displays the estimated capacitor voltage increase, and Fig. 15 (c) displays the values of CMI_{ij} based on equation (13). The great accuracy of the suggested monitoring approach is demonstrated by the *CMI* values for C_{u11} and C_{u12}, which are $CMI_{u11}=0.75 \pm 0.2\%$ and $CMI_{u12}=0.8 \pm 0.4\%$, respectively. In this approach, if the damaged capacitor oscilloscope. Table 7 lists other critical parameters of the experimental setup. In this approach, if the damaged capacitor and keeps the MMC from further dangers. Additionally, the suggested monitoring technique ensures the capacitor voltage estimate method's excellent accuracy.

VI. Experimental evaluation

After the initial evaluation with different simulation scenarios, the proposed methods are implemented on a 5-level low-scale laboratory sample**.** Fig. 16 shows the experimental setup using four half-bridge sub-modules in each arm. According to the voltage sensor arrangement in this paper, two voltage sensors are required for each arm to manage the voltage balance of the capacitors. Also, the proposed methods and all MMC control algorithms have been implemented using Code Composer software and the JTAG interface on a TMS320F2812 DSP processor. Dual output drivers with IRF640N MOSFETs have been used in the laboratory setup structure for switching operations to increase the output signals sent from the microcontroller up to 15V. Also, all figures in experimental studies have been extracted to TIF format using a Tektronix DPO 5034 oscilloscope. Table 7 lists other critical parameters of the experimental setup.

A. Performance of steady-state conditions

Fig. 17 shows the experimental performance results of the proposed capacitor voltage estimation method under steady-state conditions. As shown in Fig. 17 (a), the output voltage is well produced at 5-level with the least disturbance. Fig.

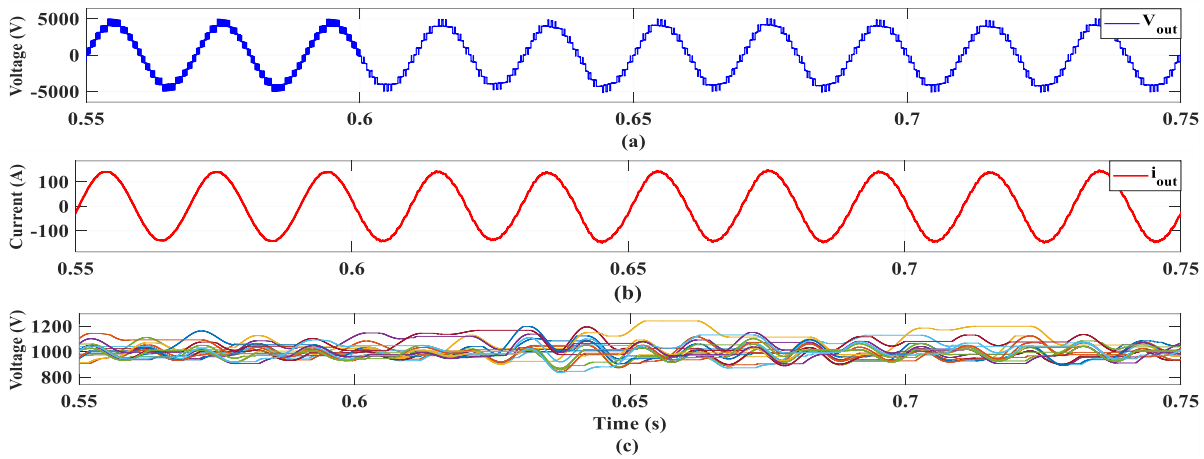

Fig. 11. Simulation results in transient conditions (Reference method) (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage

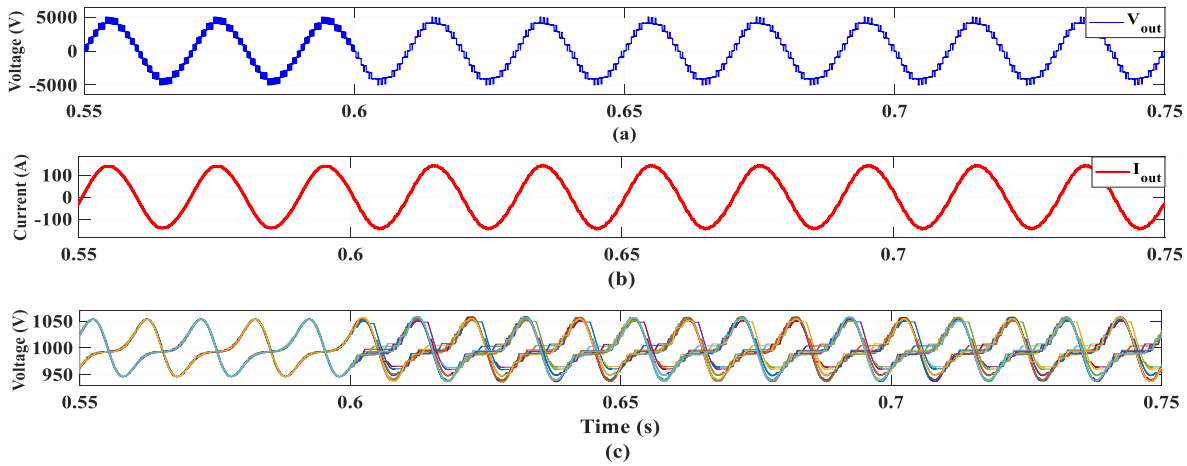

Fig. 12. Simulation results in transient conditions (proposed estimation method) (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage

17 (b) also displays the current on the AC side, which oscillates with the least total harmonic distortion and in a sinusoidal pattern with a fundamental frequency of 50 Hz. Fig. 17 (c) depicts the capacitor voltage of the upper arm sub-modules, which oscillates at the capacitors' nominal voltage (30V) with a ripple of roughly 5% V_{nam}.

B. Performance by changing the modulation index

In this case, the converter is initially operating in a steady-state. At t = 1.08s, M_a decreases from 0.9 to 0.4; as shown in Fig. 18 (a) and Fig. 18 (b), the terminal voltage of the AC side is reduced from 5 to 4 levels, and the current range of the AC side is decreased from 1.9A to 0.8A. Despite the sudden change in M_a, the voltages of capacitors remain balanced (Fig. 18 (c)). Therefore, the proposed estimation method shows excellent performance. At t = 1.18s, the M_a changes once more to its steady-state value. Fig. 19 shows a scenario where the load impedance at t = 1.1s undergoes a sudden increase of 100%. Notably, notwithstanding the precipitous decline in the output current, the capacitors' voltage balance control is adeptly sustained. This observation attests to the efficacy of the employed estimation method, underscoring its capability to ensure proper system performance in the face of load impedance variations. To scrutinize the robustness of the proposed method, an examination was conducted under extreme conditions. Specifically, the intentional reduction of the DC link voltage from 120 V to 40 V is depicted in Fig. 20 within the experimental results for this scenario. Figures 20 (a) and 20 (b) vividly illustrate a sudden and substantial decline in both output voltage and current in response to the diminished DC link voltage. Nevertheless, the balance control and capacitors are well maintained.

C. Performance of the proposed monitoring method

Evaluation of the accuracy of the proposed monitoring method has been done by examining the capacitance of SM_{u12}. By using the LCR meter, the capacitance of C_{u12} is measured to be 1549 µF, instead of the nominal 2200 µF. As a result, CMI_{u12}=0.704 represents the capacitance monitoring index's true value. The experimental

performance results of the method proposed are shown in Fig. 21. The measured voltage rise is equal to 1.91V, as shown in Fig. 21 (a). Also, by using the graph feature of processor, an estimated voltage increases of 1.35V is shown in Fig. 21 (b). The proposed capacitance monitoring index is equal to CMI_{u12}=0.706. As a result, the proposed monitoring method is able to accurately monitor the capacitance in MMC with an error of about 1%, which indicates the optimal performance of the proposed method despite the reduced number of sensors.

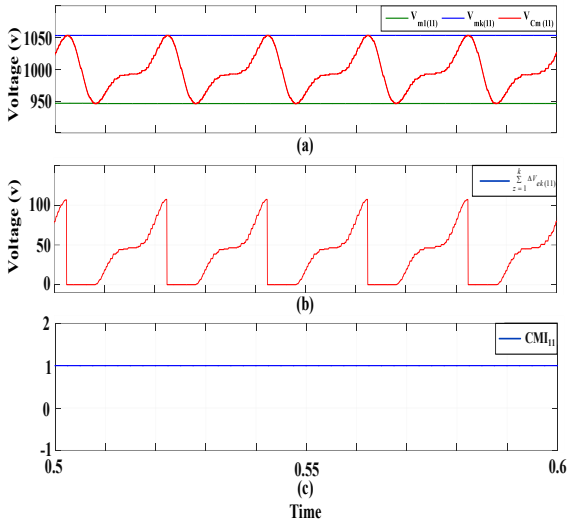

Fig. 13. Simulation results of the monitoring method for C_{u11} (a) Measured voltage increase, (b) Estimated capacitor voltage increase, (c) CMI_{u11} value.

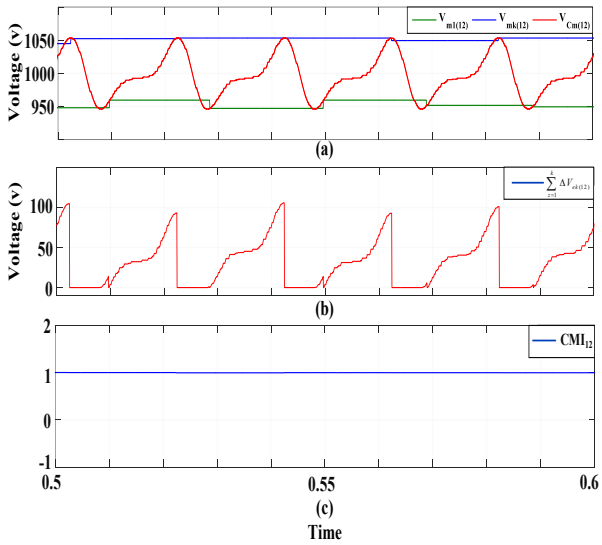

Fig. 14. Simulation results of the monitoring method for C_{u12} (a) Measured voltage increase, (b) Estimated capacitor voltage increase, (c) CMI_{u12} value.

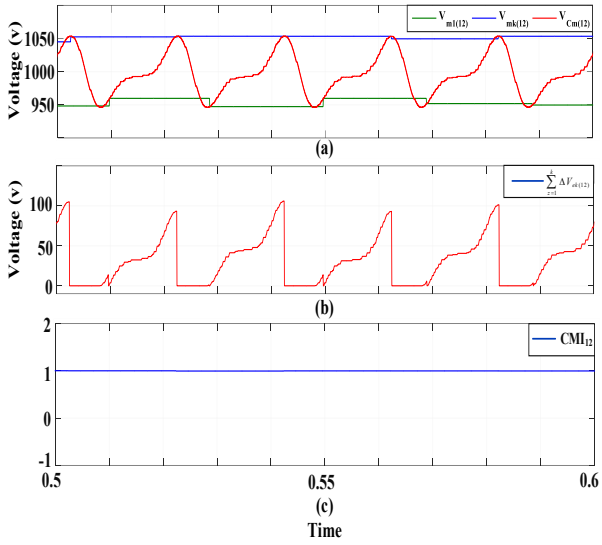

Fig. 15. Simulation results of the monitoring method for C_{u12} (a) Measured voltage increase, (b) Estimated capacitor voltage increase, (c) CMI_{u12} value.

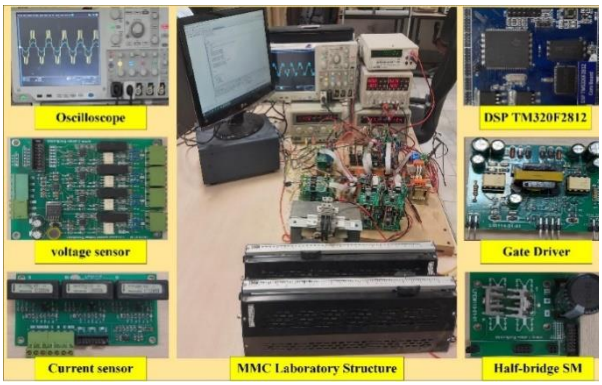

Fig. 16. MMC experimental-setup.

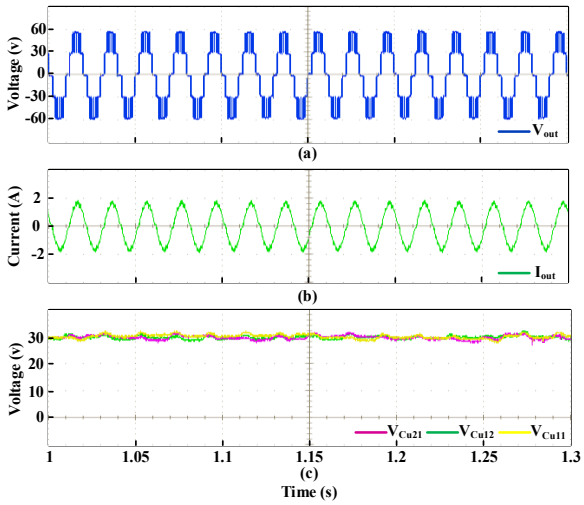

Fig. 17. Experimental results in steady-state conditions. (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage.

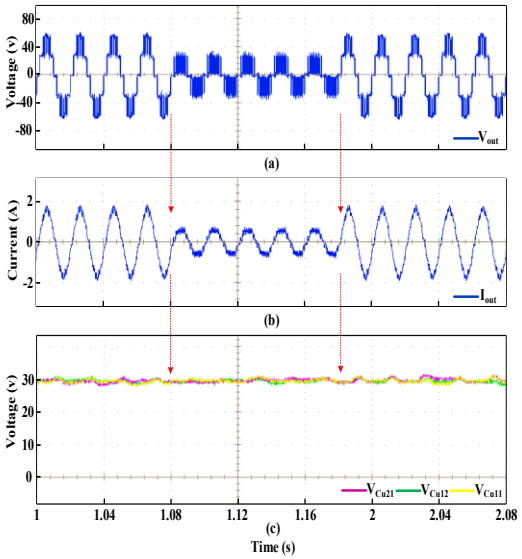

Fig. 18. Experimental results in transient state conditions (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage.

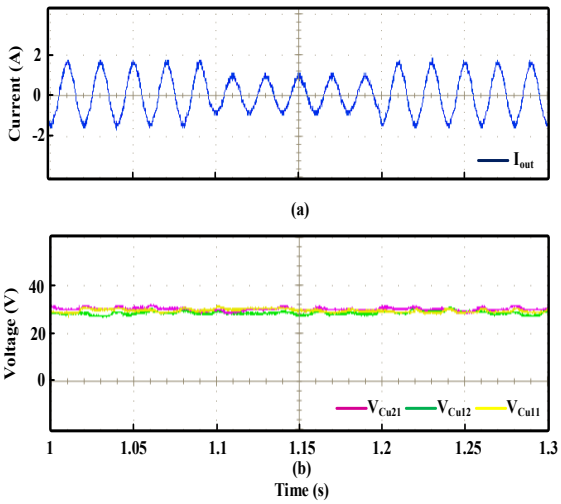

Fig. 19. Experimental results in transient state conditions (a) AC-side current, (b) HB-SMs voltage.

VII. Conclusion

This study presents an improved capacitor voltage balancing method that offers several key advantages for high-voltage and high-power MMC applications. The developed strategy effectively addresses the critical challenge of managing the large number of flying capacitors in the converter. Compared with conventional solutions, employing a single voltage sensor for two half-bridge submodules reduces the required sensor count while simultaneously improving computational efficiency and overall system reliability. The introduced estimation approach eliminates the need for forced activation algorithms or correction factors, making the control process simpler and more robust.

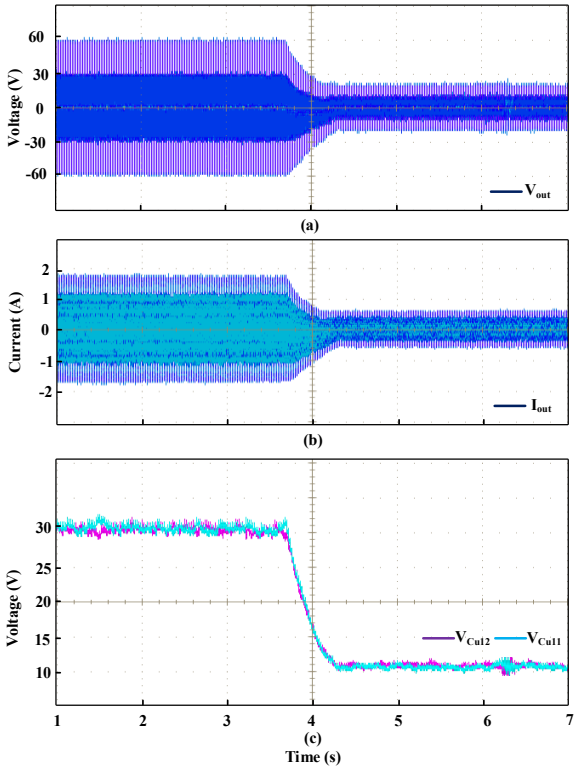

Fig. 20. Experimental results in transient state conditions (a) AC-side voltage, (b) AC-side current, (c) HB-SMs voltage.

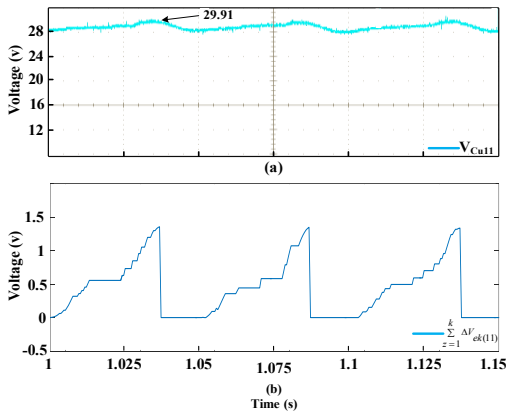

Fig. 21. Experimental results of the monitoring method for Cu12 (a) Measured voltage increase, (b) Estimated capacitor voltage increase.

In addition, a novel capacitance monitoring technique has been demonstrated, enabling accurate health assessment of capacitors once per cycle with less than 1% error. This capability significantly enhances the reliability and fault tolerance of the converter. Both simulation and experimental investigations confirm the effectiveness of the presented methods across steady-state and transient conditions. The results highlight that the developed approach is not only accurate and computationally efficient but also practical for real-world high-power and high-voltage applications.

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