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Improved Symmetric Switched-Inductor/Capacitor Quasi Z-Source Inverter with Ability Uplifted-Boost

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ABSTRACT

This paper proposes a topology of switched-inductor/capacitor quasi z-source inverter (SIC-qZSI) based on the classic qZSI. This topology is symmetric with a high boost factor in the low duty cycle and high modulation index, the low voltage stress on the capacitors, and the low current of the inductors and the input source. In addition, the current of all inductors and the input current are equal, and the voltage across all the inductors, as well as the voltage across all diodes, are equal. The performance of the proposed topology is confirmed with MATLAB/SIMULINK software and the simulation results and obtained relations are certified by using a prototype of the proposed inverter.

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I. INTRODUCTION

With the advancement of technology, the inverters have found a vital role in the industry. In spite of the wide application of the voltage source inverter (VSI) and the current inverter (CSI) in the industry, these inverters have major disadvantages [1], [2], [3]. Therefore, they require a two-stage conversion to have both Boost's and buck's capabilities that the cost increases due to the additional converter [4]. Also, creating dead time to prevent the short circuit of the input voltage source, and the vulnerability to EMI noise, are another disadvantages of these inverters that reduce the reliability of the inverter [5]. In 2003, the impedance source inverter (ZSI) was suggested which could overcome the VSI and CSI problems [6]. The impedance□source network idea has opened up a novel research area in the power electronics [7]. This topology is used in the all stages of the power conversion (ac-ac, dc-ac, dc-dc, ac-dc) with buck and boost capability [6], [8], [9]. The impedance-source inverter (ZSI) can increase the voltage gain in one step with shoot-through states while they do not need the additional dc-dc converter [10]. Therefore, by elimination dead time in order to avoid the short circuit of the voltage source, as well as the non-vulnerability of the converter to EMI noise, the inverter reliability increases [11], [12]. Use of ZSI instead of VSI in the traditional general-purpose motor drive (or adjustable speed drive-ASD) based on VSI, resulted in improved performance and fixing its disadvantages [13]. Despite the significant advantages of these inverters compared to VSI and CSIs, they have disadvantages such as high voltage stress on capacitors and switching devices, discontinuous input current, and lack of common ground between the input source and the bridge inverter. In 2008, the improved ZSI topology was introduced which compared to conventional ZSI possess lower voltage stress on impedance network capacitors with the same boost factor, as well as, inherent limitation to inrush current at startup [14]. Photovoltaic systems (PV) with a clearer view, high reliability, low operating cost, Eco-friendly and easier maintenance of renewable energy has been more consideration [15]. Because of the input inductor, the quasi-impedance source inverter (qZSI) draws a continuous constant DC current from the DC input source. Compared with the ZSI, which draws a discontinuous current, the constant current will significantly reduce input stress; the qZSI with continuous input current is especially well suited to PV system applications. Continuous input current, common ground between input source and inverter bridge, and low voltage stress on capacitors are among the advantages of a qZSI compared with traditional ZSI in the same voltage boost [16].

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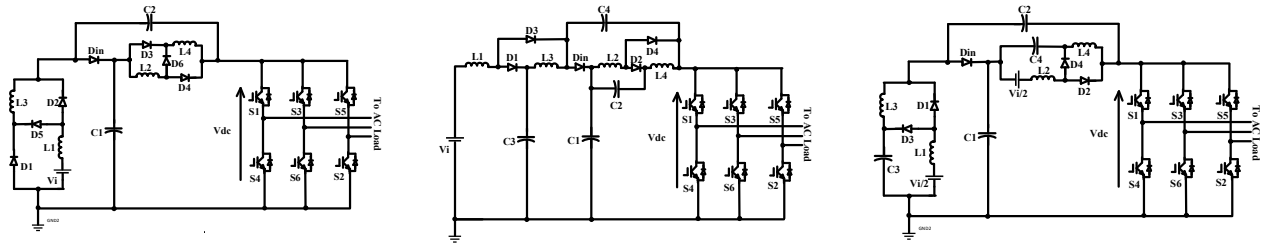


(a) (b) (c)

Fig. 1. Topology compared with the proposed topology; (a) cSL-qZSI [20], (b) Enhanced-boost qZSI (EB-qZSI) [22], (c) ESL-qZSI [10].

In Ref [17] the diode assisted qZSI (DA-qZSI) and capacitor-assisted qZSI (CA-qZSI) topologies have been offered possessing higher voltage boost and lower voltage stress on capacitors and diodes. Also, the other benefit of these topologies is their extensibility. In 2010 and 2011, switched-inductor Z-source inverter (SL-ZSI) and switched-inductor quasi Z-source inverter (SL-qZSI) topologies were proposed wherein, the switched-inductor cells were used instead of inductors in the ZSI/qZSI structures resulted in a significantly increased Boost factor. However, SL-ZSI has a higher boost ratio than SL-qZSI, but the SL-qZSI have advantages such as common ground between the input source and inverter bridge and lower stress on capacitors [18], [19]. The startup inrush current of the converters damages the devices. The suppress of the startup inrush current and the lower voltage stress on the capacitors are the benefits of the continuous input current switched-inductor quasi-Z-source inverter (cSL-qZSI) compared with the above mentioned structures. Fig. 1(a) shows the structure of cSL-qZSI [20]. In 2016, enhanced boost-qZSI (EB-ZSI) topology was suggested that has a high boost factor at low shoot through duty ratio and high modulation index. However, it have disadvantages such as, the lack of common ground between the input source and the inverter bridge, as well as, discontinuous input current [21]. The topology of the enhanced boost-qZSI (EB-qZSI), in addition to overcoming the EB-ZSI problems, has lower voltage stress on capacitors at the same boost factor [22]. The EB-qZSI structure is shown in Fig. 1(b). In [10], the symmetric topology called embedded switched-inductor qZSI (ESL-qZSI) was suggested. The low voltage stress on the capacitors, the low ripple current of the inductors, and the high boost factor are the advantages of these structures. The ESL-qZSI structure is shown in Fig. 1(c). For better improvement the boost capability without using additional components, a three-winding switched-coupled inductor (SCL) is applied to the modified SL-qZSI and is termed as SCL-qZSI in [23], it memorizes all of the benefits of QZSI and suppresses the startup inrush current. Similarly, structures used of winding coupled inductors such as T-source [24], Trans-Z-source [25] and Y-source [26] have been introduced subsequently. Though high voltage gain is achieved, the output voltage is sensitive to the leakage inductance [12].

This paper proposes a symmetric topology that has a high boost factor in high modulation index and low duty cycle in comparison with similar structures. The low voltage stress on the capacitors and the low input current ripple is another advantages of this topology. To investigate the characteristics of the proposed inverter (SIC-qZSI), the EB-qZSI prototype has been constructed with similar elements used in the proposed inverter and their experimental results are compared.

II. PROPOSED TOPOLOGY

As can be seen from Fig. 2, the proposed topology (SIC-qZSI) consists of two switched-inductor/capacitor cells that increase the voltage of the DC link voltage (V_{PN}). This structure has four inductors(L_{1-4}), six capacitors (C_{1-6}) and three diodes(D_{1-3}). As seen in Table I, the number of elements is compared in different structures. In comparison with the EB-qZSI, this structure has two fewer diodes, but two additional capacitors.

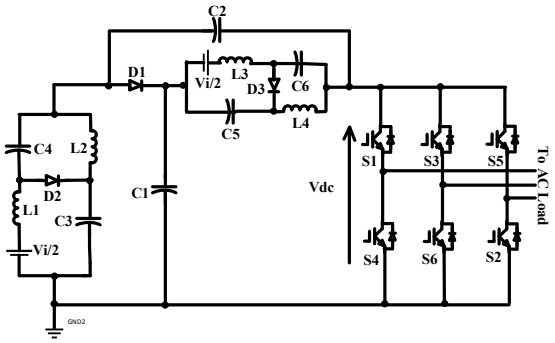


Fig. 2. Proposed topology (SIC-qZSI).

A. Circuit Analysis

The operation principles of the proposed topology are the same as the traditional ZSI/qZSI and possess shoot-through zero state, six active states, and two zero states. The zero state of shoot-through provides a unique specification of buck-boost in the impedance source inverters. For simpler analysis, the operating conditions can be considered as shoot-through (ST) and non-shoot-through states (N-ST).

TABLE I

Comparison of the number of elements used in the proposed structure with other structures

No. of components	DA-qZSI [16]	CA-qZSI [16]	SL-ZSI [18]	rSL-qZS [19]I	cSL-qZSI [19]	EB-qZSI [21]	ESL-qZSI [10]	iESL-qZSI [10]	Proposed structure
Capacitor	3	4	2	2	2	4	4	4	6
Inductor	3	3	4	4	4	4	4	4	4
Diode	3	2	7	7	7	5	5	5	3
Power switch	6	6	6	6	6	6	6	6	6

Fig. 3(a) shows the equivalent circuit of shoot through state. During ST state, both the up and down switches in each legs of main inverter are on, and D_1 and D_2 diodes are off, and unlike other topologies, none of the diodes are on. So, by writing KVL in this circuit, the following relations are obtained:

$$\begin{cases} V_{L1} = \dfrac{V_i}{2} + V_{C2} + V_{C4} \\ V_{L2} = V_{C2} + V_{C3} \\ V_{L3} = \dfrac{V_i}{2} + V_{C1} + V_{C6} \\ V_{L4} = V_{C1} + V_{C5} \\ V_{PN} = 0 \end{cases} \quad (1)$$

Also, the voltage of the diodes can be obtained in ST mode as:

$$\begin{cases} V_{D1} = -V_{C1} - V_{C2} \\ V_{D2} = -V_{C2} - V_{C3} - V_{C4} \\ V_{D3} = -V_{C1} - V_{C5} - V_{C6} \end{cases} \quad (2)$$

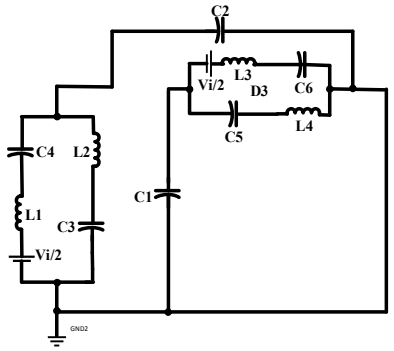


Fig. 3 (a)

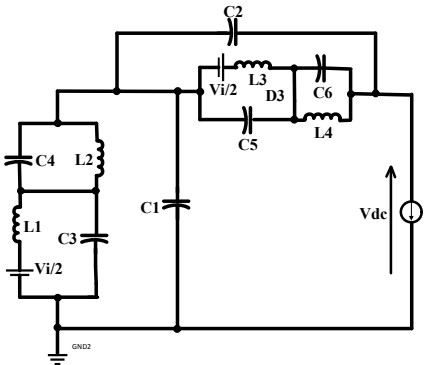


Fig. 3 (b)

Fig. 3. Equivalent circuits of the proposed topology (SIC-qZSI) (a) ST state (b) N-ST state.

As can be seen Fig. 3 (b), in N-ST state, the diodes D_1 and D_2 are on and unlike other topologies, none of the diodes are off. In this state, the inductor transfer energy to the load and the capacitor is charged through the input voltage source. Similarly, by writing KVL in this circuit, the following relations will be obtained:

$$\begin{cases} V_{L1} = \dfrac{V_i}{2} - V_{C3} = \dfrac{V_i}{2} + V_{C4} - V_{C1} \\ V_{L2} = -V_{C4} = V_{C3} - V_{C1} \\ V_{L3} = \dfrac{V_i}{2} - V_{C5} = \dfrac{V_i}{2} + V_{C6} - V_{C2} \\ V_{L4} = -V_{C6} = V_{C5} - V_{C2} \end{cases} \quad (3)$$

$$V_{PN} = V_{C1} + V_{C2} \quad (4)$$

Applying the volt-sec balance principle and under steady state condition, the average voltage of the inductors over one switching cycle is zero. So, relations of the voltage stress on capacitors can be obtained as follow:

$$V_{C1} = V_{C2} = \frac{1}{2(1-4D)} V_i \quad (5)$$

$$V_{C3} = V_{C5} = \frac{1-2D}{2(1-4D)} V_i \quad (6)$$

$$V_{C4} = V_{C6} = \frac{D}{1-4D} V_i \quad (7)$$

Considering the above relations, it can be concluded that the proposed topology is symmetric. The relation the boost factor in the proposed topology can be obtained by replacing the voltage stress relations on C_1 and C_2 capacitors in (4) as follows:

$$B = \frac{V_{PN}}{V_i} = \frac{1}{1-4D} \quad (8)$$

According to the Table II, the comparison between boost factor relations of the suggested topology with other topologies have been carried out indicating the higher boost factor of the proposed topology than the other structures in the same input voltage and shoot-through duty cycle. Therefore, at the suggested topology in shoot through duty cycle 0.15, 0.2 and 0.23, the boost factors increase to 2.5, 5 and 12.5, respectively. Fig. 4 compares the boost factor of different topologies with the proposed topology. As can be seen, the proposed structure has a higher boost factor than other structures under equal conditions with the same number of elements.

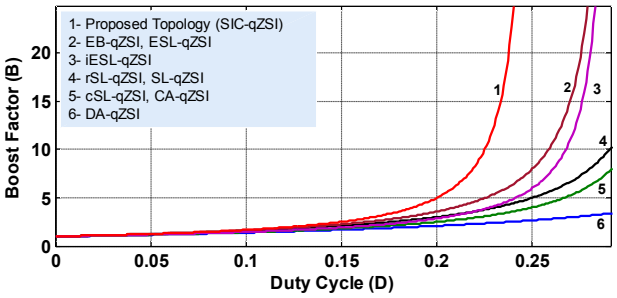


Fig. 4. Comparison of the boost factor (B) of different Z-source topologies with the proposed topology (SIC-qZSI).

B. PWM Technique and Voltage Gain

Several control techniques exist for controlling switches in various ZSI topologies, such as the simple boost control [27], [16], phase-shift control [29]-[30] , the maximum boost control [31] and the constant maximum boost control methods [32] that purpose is attain wide area of modulation, simple implementation, loss of commutation for each switching cycle, and low stress on system. The relationship between M and B depends on the type of PWM control strategy. In the proposed topology, simple boost control technique has been applied. This technique is like the conventional sinusoidal PWM method, with the difference that two constant signals of the positive amount (V_p) and negative amount (V_n) have been added to produce the shoot-through state. These signals can be larger or equal to the positive peak of the sinusoidal reference waves, or can be smaller or equal to the negative peak of the sinusoidal reference waves. To obtain the peak-phase output voltage in three-phase inverters, the following relation can be used:

$$v_{an,max} = M.\frac{V_{PN}}{2} \tag{9}$$

Where, M is the amplitude modulation index.

By substituting relationship (8) in (9), the peak-phase output voltage toward the boost factors (B) can be derived as:

$$v_{an,max} = M.B\frac{V_i}{2} \tag{10}$$

Given the relation (10), the multiplication of M.B is called the voltage gain (G) of inverter. As regards to the simple boost PWM control method, modulation index (M) relative to the shoot-through duty cycle (D), is 1-D. So, the voltage gain (G) relative to M in the suggested topology can be obtained as follows:

$$G = \frac{M}{4M-3} \tag{11}$$

Fig. 5 shows the voltage gain versus modulation index for different topologies. As can be seen, voltage gain of the proposed SIC-qZSI is higher than that of all the comparative topologies at the same input voltage and shoot-through duty cycle.

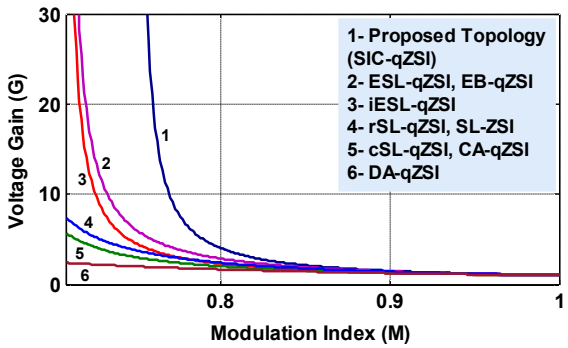


Fig. 5. Comparison of the voltage gain of proposed topology (SIC-qZSI) with other topologies.

C. Comparison of Voltage Stress on Capacitors and Diodes

Power electronic converters with low voltage stress reduce capacitor rating, that's the size and cost of the converter is reduced [33]. Since the proposed topology ($SIC\text{-}qZSI$) is symmetric, the voltage stresses of the corresponding capacitors in both the switched-inductor/capacitor cells are equal. Accordingly, C_3 voltage stress with C_5, C_4 with C_6, as well as, the voltage stress of the impedance network capacitors which means C_1 with C_2 are equal. Voltage stress on capacitors is obtained from relations (5), (6) and (7). According to Fig. 6, the voltage stress of the proposed topology capacitors ($SIC\text{-}qZSI$) is compared with the two conventional topologies of $EB\text{-}qZSI$ and $ESL\text{-}qZSI$ with the same number of elements.

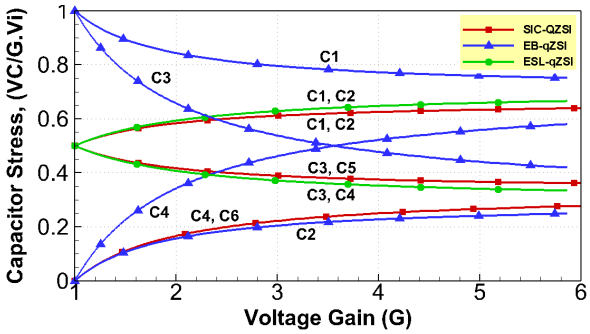


Fig. 6. Comparison of voltage stresses of proposed topology (SIC-qZSI) capacitors with Enhanced boost-qZSI and ESL-qZSI.

As can be seen, the voltage stress of the capacitors in the impedance network (C_1, C_2) and switched-inductor/capacitor cells (C_{3-6}) of the proposed topology, are almost lower than the $ESL\text{-}qZSI$ topology. Compared to the $EB\text{-}qZSI$ topology, in the impedance network, the capacitor C_2 has lower voltage stress, while C_1 has higher voltage stress relative to the corresponding capacitors in the proposed topology. However, switched-inductor/capacitor cell capacitors of the proposed topology have lower voltage stress than the corresponding capacitors in the $EB\text{-}qZSI$ structure. According to Fig. 7, the voltage stress on the proposed

topology diodes is greater than the *EB-qZSI* and *ESL-qZSI* structures. However, voltage stress is equal in all diodes of the proposed structure.

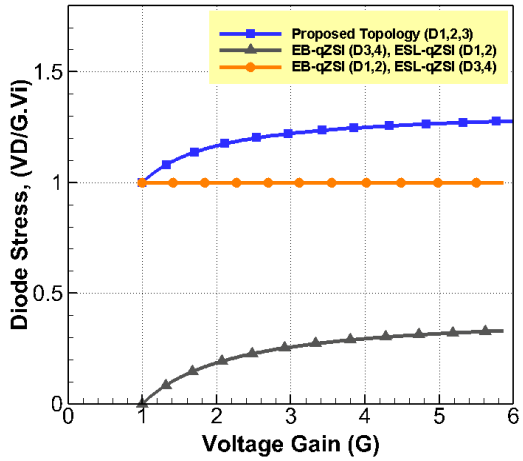


Fig. 7. Comparison of voltage stresses of proposed topology (SIC-qZSI) diodes with Enhanced boost-qZSI and ESL-qZSI.

D. Current Ripple of Inductors and Voltage Across Inductors

The relation between the voltages across of the inductor with the current through it, is obtained from equation (12).

$$V_L = L\frac{di}{dt} \tag{12}$$

By replacing the voltage stress of the capacitors in (1) and (3), the voltage across the inductors in the ST and non-ST states, respectively, are calculated as follows:

$$V_{L1} = V_{L2} = V_{L3} = V_{L4} = \frac{1-D}{1-4D} \tag{13}$$

$$V_{L1} = V_{L2} = V_{L3} = V_{L4} = \frac{-D}{1-4D} \tag{14}$$

By replacing the relations (13) and (14) in (12), the current ripple of the inductors for ST and non-ST states, are calculated as:

$$\Delta i_i = \Delta i_{L1} = \Delta i_{L2} = \Delta i_{L3} = \Delta i_{L4} = \frac{D(1-D)}{2Lf(1-4D)}V_i \tag{15}$$

$$\Delta i_i = \Delta i_{L1} = \Delta i_{L2} = \Delta i_{L3} = \Delta i_{L4} = \frac{-D(1-D)}{2Lf(1-4D)}V_i$$

$$\Delta i_i = \Delta i_{L1} = \Delta i_{L2} = \Delta i_{L3} = \Delta i_{L4} = \frac{-D(1-D)}{2Lf(1-4D)}V_i \tag{16}$$

Given the relation (16), the inductance is obtained as follows:

$$L = \frac{D(1-D)}{(1-4D)}.\frac{V_i}{2f\Delta i} \tag{17}$$

It is assumed that the inverter is ideal, the output power and inverter input are equal. Consequently, in the pure resistance load, the input current will be equal to the following relation:

TABLE II

Comparison of voltage stress on capacitors, inductors current ripple, diode stress, boost factor voltage gain, in proposed topology (sic-qzsi) with other topologies.

	Parameter	CA-qZSI	SL-ZSI	cSL-qZSI	rSL-qZSI	EB-qZSI	ESL-qZSI	iESL-qZSI	Proposed Structure
Capacitors Stress	C_1	$\frac{D}{1-3D}V_i$	$\frac{1-D}{1-3D}V_i$	$\frac{1-D}{(1+D)(1-3D)}V_i$	$\frac{1-D}{1-3D}V_i$	$\frac{(1-D)^2}{1-4D+2D^2}V_i$	$\frac{1}{2(1-4D+2D^2)}V_i$	$\frac{1-D}{2(1-4D+2D^2)}V_i$	$\frac{1}{2(1-4D)}V_i$
	C_2	$\frac{D}{1-3D}V_i$	$\frac{1-D}{1-3D}V_i$	$\frac{2D}{(1+D)(1-3D)}V_i$	$\frac{2D}{1-3D}V_i$	$\frac{D(1-D)}{1-4D+2D^2}V_i$	$\frac{1}{2(1-4D+2D^2)}V_i$	$\frac{1-D}{2(1-4D+2D^2)}V_i$	$\frac{1}{2(1-4D)}V_i$
	C_3	$\frac{1-2D}{1-3D}V_i$	Not exist	Not exist	Not exist	$\frac{1-3D+D^2}{1-4D+2D^2}V_i$	$\frac{1-2D}{2(1-4D+2D^2)}V_i$	$\frac{D}{2(1-4D+2D^2)}V_i$	$\frac{1-2D}{2(1-4D)}V_i = V_{C5}$
	C_4	$\frac{D}{1-3D}V_i$	Not exist	Not exist	Not exist	$\frac{D(2-D)}{1-4D+2D^2}V_i$	$\frac{1-2D}{2(1-4D+2D^2)}V_i$	$\frac{D}{2(1-4D+2D^2)}V_i$	$\frac{D}{1-4D}V_i = V_{C6}$
Current Ripple	L_1	$\frac{D(1-D)}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D^2}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{2D^2}{(1+D)(1-3D)}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)^2}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)^2}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D}{2(1-4D+2D^2)}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D}.\frac{V_i}{2Lf_s}$
	L_2	$\frac{D(1-D)}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D^2}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{(1+D)(1-3D)}.\frac{V_i}{2Lf_s}$	$\frac{D^2(1-D)}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)^2}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)^2}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D}{2(1-4D+2D^2)}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D}.\frac{V_i}{2Lf_s}$
	L_3	$\frac{(1-D)^2}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D^2}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{2D^2}{(1+D)(1-3D)}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)^2}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D}.\frac{V_i}{2Lf_s}$
	L_4	Not exist	$\frac{D^2}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{(1+D)(1-3D)}.\frac{V_i}{2Lf_s}$	$\frac{D^2(1-D)}{1-3D}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)^2}{1-4D+2D^2}.\frac{V_i}{2Lf_s}$	$\frac{D(1-D)}{1-4D}.\frac{V_i}{2Lf_s}$
Diode Stress	D_1, D_2	$\frac{-1}{1-3D}V_i$	$\frac{-D}{1-3D}V_i$	$\frac{D-1}{2(1+D)(1-3D)}V_i$	$\frac{-D}{1-3D}V_i$	$\frac{D-1}{1-4D+2D^2}V_i$	$\frac{-D}{1-4D+2D^2}V_i$	$\frac{-1}{1-4D+2D^2}V_i$	$\frac{-1}{1-4D}V_i = V_{D1,2,3}$
	D_3, D_4	Not exist	$\frac{-D}{1-3D}V_i$	$\frac{-D}{(1+D)(1-3D)}V_i$	$\frac{-D}{1-3D}V_i$	$\frac{-D}{1-4D+2D^2}V_i$	$\frac{D-1}{1-4D+2D^2}V_i$	$\frac{-1}{2(1-4D+2D^2)}V_i$	Not exist
	D_5, D_6	Not exist	$\frac{D-1}{1-3D}V_i$	$\frac{-2D}{(1+D)(1-3D)}V_i = \frac{-2DV_{D6}}{1-D}$	$\frac{D-1}{1-3D}V_i$	$\frac{-D}{1-4D+2D^2}V_i$	Not exist	Not exist	Not exist
	Boost Factor	$\frac{1}{1-3D}$	$\frac{1+D}{1-3D}$	$\frac{1}{1-3D}$	$\frac{1+D}{1-3D}$	$\frac{1}{1-4D+2D^2}$	$\frac{1}{1-4D+2D^2}$	$\frac{1-D}{1-4D+2D^2}$	$\frac{1}{1-4D}$
	Voltage Gain	$\frac{M}{2M-2}$	$\frac{M(2-M)}{3M-2}$	$\frac{M}{3M-2}$	$\frac{M(2-M)}{3M-2}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M^2}{2M^2-1}$	$\frac{M}{4M-3}$

$$i_i = i_{L1} = i_{L2} = i_{L3} = i_{L4} = \frac{3(1-D)^2}{(1-4D)^2} \cdot \frac{V_i}{8R} \quad (18)$$

The above relations show that in the proposed topology unlike other topologies, all inductors have equal voltage, current, and current ripple. If K_I is defined as the coefficient of the inductor current ripple, then:

$$K_I = \frac{D(1-D)}{1-4D} \quad (19)$$

The coefficient of inductor current ripple versus boost factor is shown in Fig. 8. As can be seen, the inductor current ripple rises with the boost factor increase. Therefore, under the same conditions, the current ripple is lower in all of the proposed topology inductors relative to the current ripple of the inductors L_3 and L_4 on both topologies $ESL\text{-}qZSI$ and $EB\text{-}qZSI$. But, they are larger than the current ripple of the inductors L_1 and L_2.

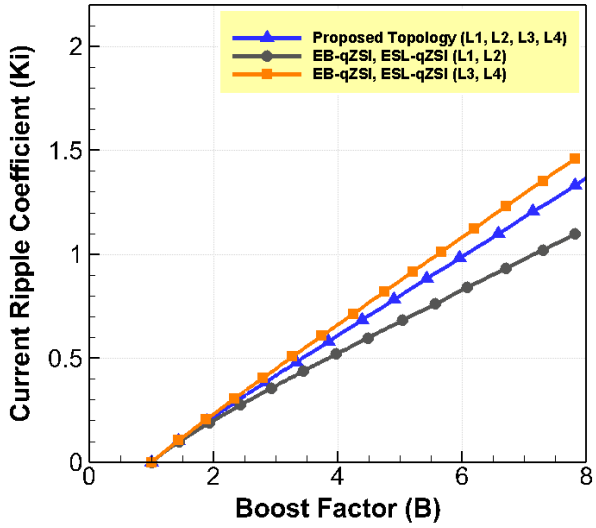


Fig. 8. Comparison of current ripple coefficient versus Boost Factor of proposed topology $(SIC\text{-}qZSI)$ inductors with $EB\text{-}qZSI$ and $ESL\text{-}qZSI$.

III. SIMULATION RESULTS

To investigate and accredit the relations obtained form the proposed topology $(SIC\text{-}qZSI)$, using the $MATLAB/SIMULINK$ software, the proposed inverter is simulated at $D = 0.2, V_i = 48V, R = 47\Omega$. According to Fig. 2, the proposed topology has high boost factor. For instance, at $D = 0.2$, the boost factor is equal to five $(B = 5)$. Given the symmetry of the proposed structure, the capacitors C_1, C_3, C_4 are equal to their corresponding capacitors namely, C_2, C_5, C_6, respectively.

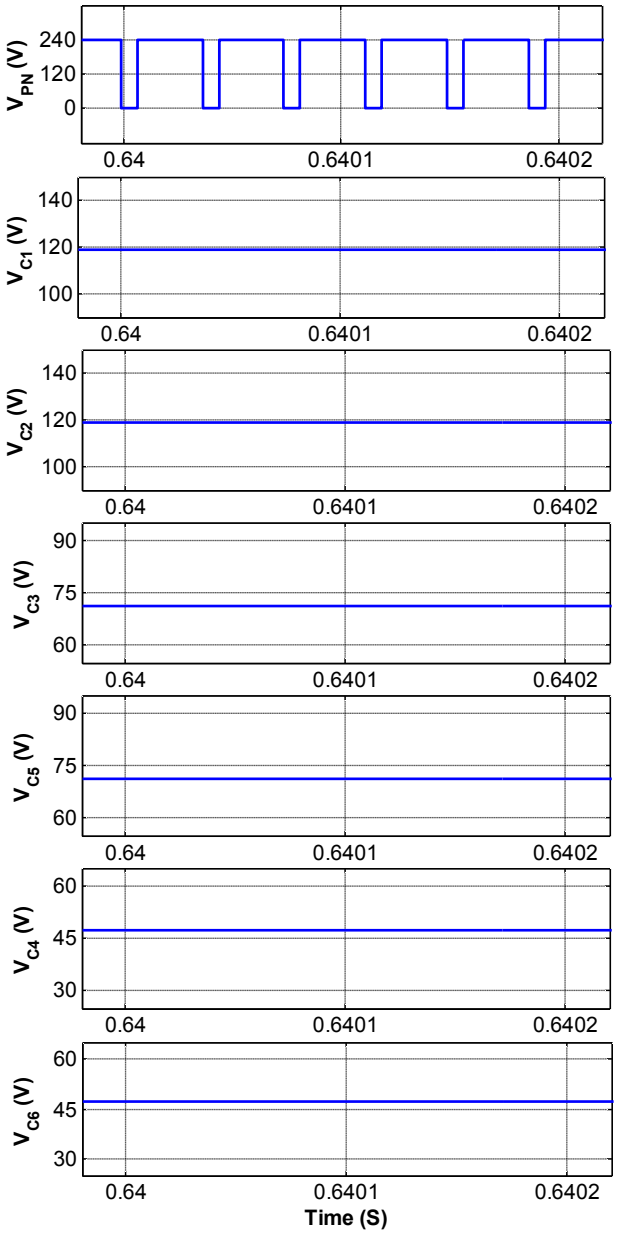
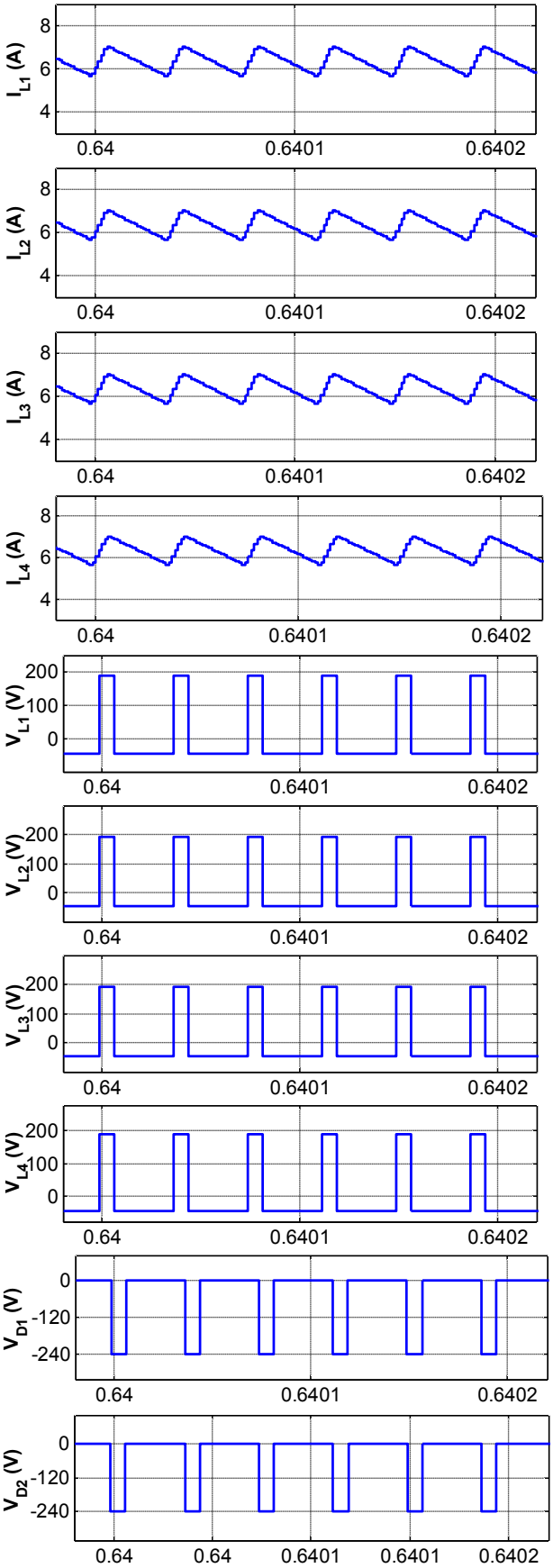


Fig. 9. The simulation results of the proposed topology (SIC-qZSI) with, $V_i = 48V$, $M = 0.8$ and $D = 0.2$. From top to bottom: DC-link voltage (V_{PN}), voltage stresses on capacitors $(C_1, C_2, C_3, C_5, C_4, C_6$ respectively).

Fig. 10 shows that the current ripple, current, and the voltage across all the inductors are equal, as well as, the stress on all diodes is equal. As can be seen, under the given conditions $(V_i = 48V, M = 0.8$ and $D = 0.2)$, the average current of the inductors is, $6.1A$, and the current ripple is, $1.4A$. The voltage across the inductors in the ST and non-ST states, are $190V$ and $-48V$, respectively. Also, voltage stress on diodes is 240V, which is equal to the maximum DC-link voltage (V_{dc}).



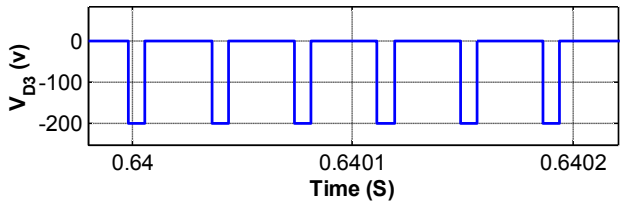


Fig. 10. The simulation results of the proposed topology (SIC-qZSI) with, $V_i = 48V$, $M = 0.8$ and $D = 0.2$. From top to bottom: inductors current (I_{L1-4}), voltage across of inductors (L_{1-4}), and voltage across of diodes(D_1, D_2).

Fig. 11 shows the line voltage, voltage and load current. The maximum line-voltage before the three-phase LC filter (V_{AB}) is $240V$, and the peak value of this voltage after the filter (V_{ab}) is approximately $160V$. Therefore, the voltage and load current are $95V$ and $2A$, respectively. Also, the output current waveform under transient load changes, it can be seen that the proposed inverter (SIC-QZSI) has a good dynamic response. The simulation result under transient resistor load changes from 47 Ω to 30 Ω, is obtained.

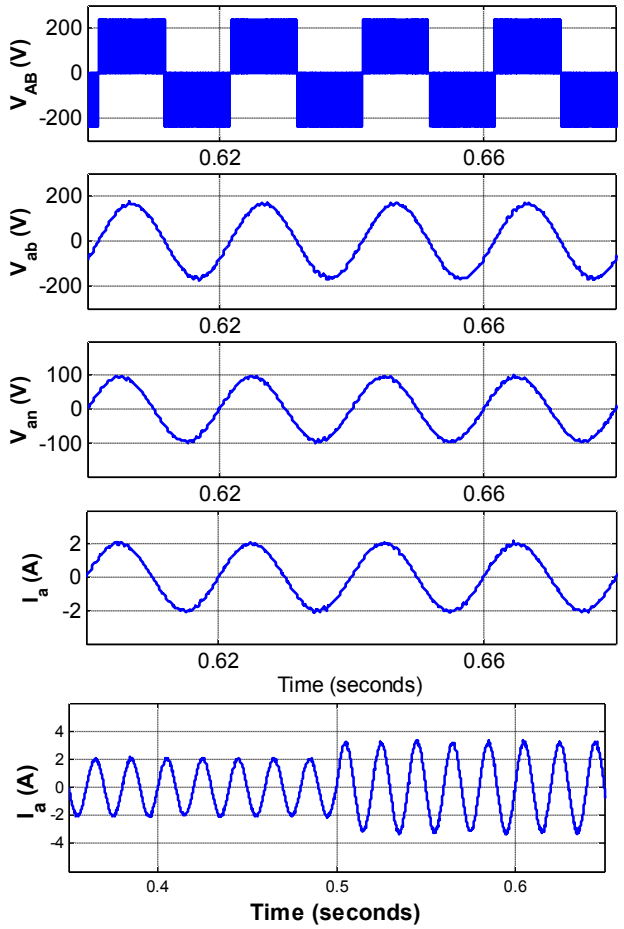


Fig. 11. The simulation results of the proposed topology (SIC-qZSI) with, $V_i = 48V$, $M = 0.8$ and $D = 0.2$. From top to bottom: Line-voltage before three phase LC filter (V_{AB}), Line-voltage after three phase LC filter (V_{ab}), and load voltage and current(V_a, I_a), simulation result under transient resistor load changes from 47 Ω to 30 Ω.

IV. Experimental results

In order to evaluate and validate the simulation results and obtained relations, the laboratory prototype of the proposed topology was constructed and the results are taken for $V_{in} = 48\,V$, $D = 0.2$ and $M = 0.8$. Figure (12) shows the laboratory prototype of the proposed topology.

A. Experimental Results of Proposed Topology

According to Fig. 13, the DC-link voltage is 220V, and the average value of the input current and its current ripple is about 5A and 1.3A, respectively. Also, the voltage stress on capacitors (C_{1-6}) are about $100V, 95V, 62V, 60V, 38V$ and $34V$, respectively, which are in good agreement with the simulation values and the obtained relationships.

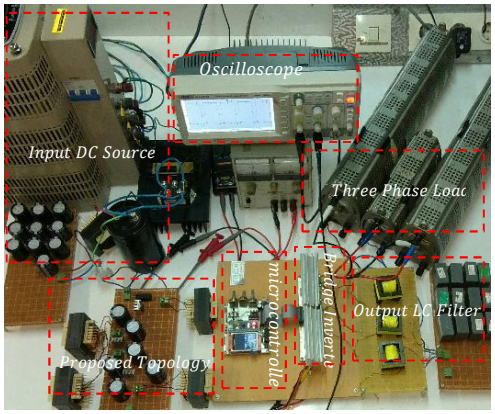
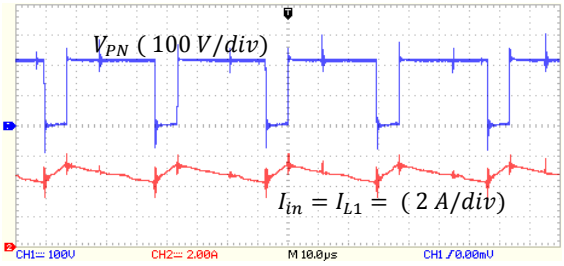
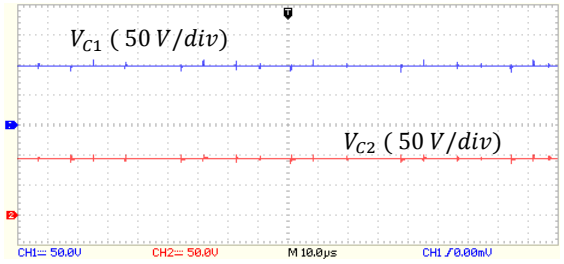
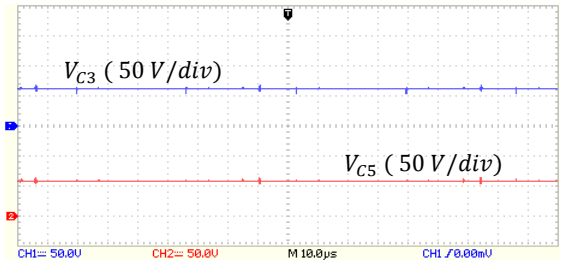


Fig. 12. Photograph of experimental setup







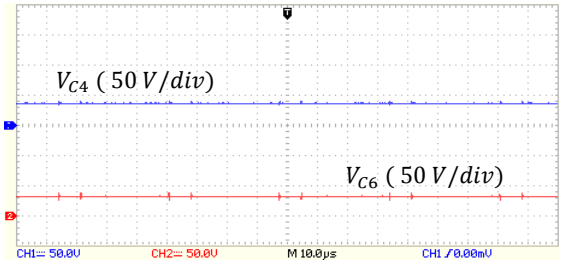
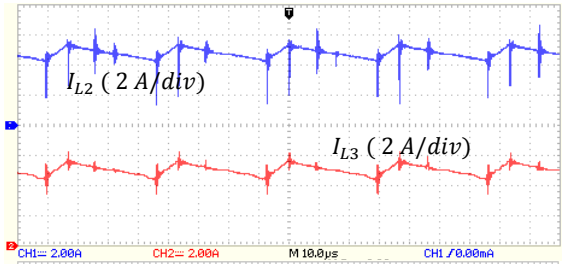
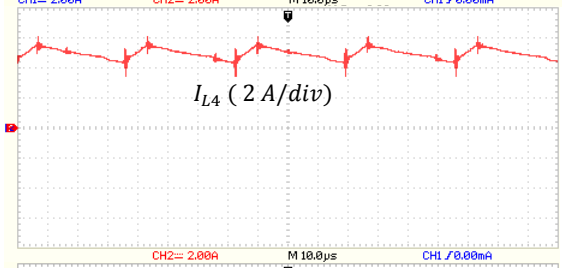
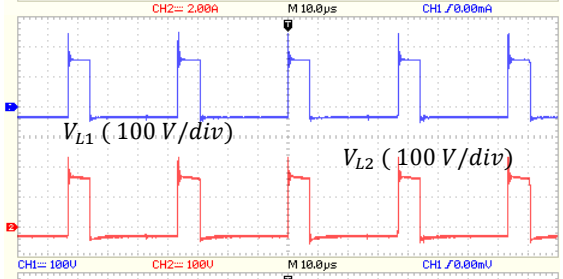


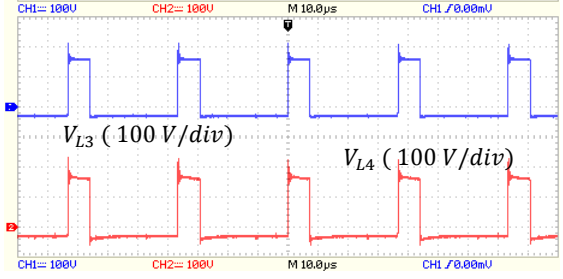
Fig. 13. The experimental results of the proposed topology (SIC-qZSI) with, $V_i = 48V$, $M = 0.8$ and $D = 0.2$. From top to bottom: DC-link voltage (V_{PN}), input current (I_i), voltage stresses on capacitors (C_{1-6}) respectively.

According to Fig. 14, the values obtained from the experimental results show that the average current and current ripple of all inducers are equal and is similar to the values obtained for the input current. The voltage in all the inductors in ST and non-ST modes is approximately $160V$ and $40V$, respectively. Also, voltage stress on diodes $D_{1,2}$ is approximately 200V.









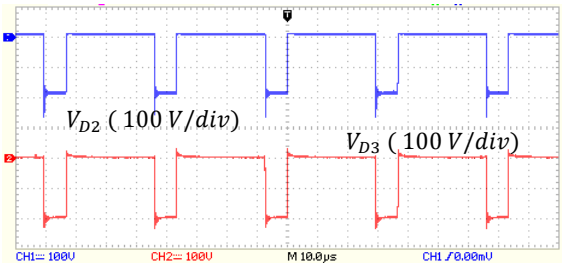


Fig. 14. The experimental results of the proposed topology (SIC-qZSI) with, $V_i = 48V$, $M = 0.8$ and $D = 0.2$. From top to bottom: inductors current (I_{L2-4}), voltage across of inductors (L_{1-4}), and voltage across of diodes(D_1, D_2).

As seen in Fig. 15, the peak of the line-voltage before and after the three-phase LC filter are $135V$ and $220V$ respectively. The peak of the voltage and load current are $85V$ and $1.5A$, respectively. Therefore, the output power under this conditions, $V_i = 48V$, $M = 0.8$ and$D = 0.2$ is approximately, $200W$. The experimental results obtained are in good agreement with the obtained equations and the simulation results and confirm them. The value of THD for output voltage and current under the resistive load are shown in Figures 15 (c) and (d), respectively, that is 6.76% for the output voltage and 7.23% for the output current.

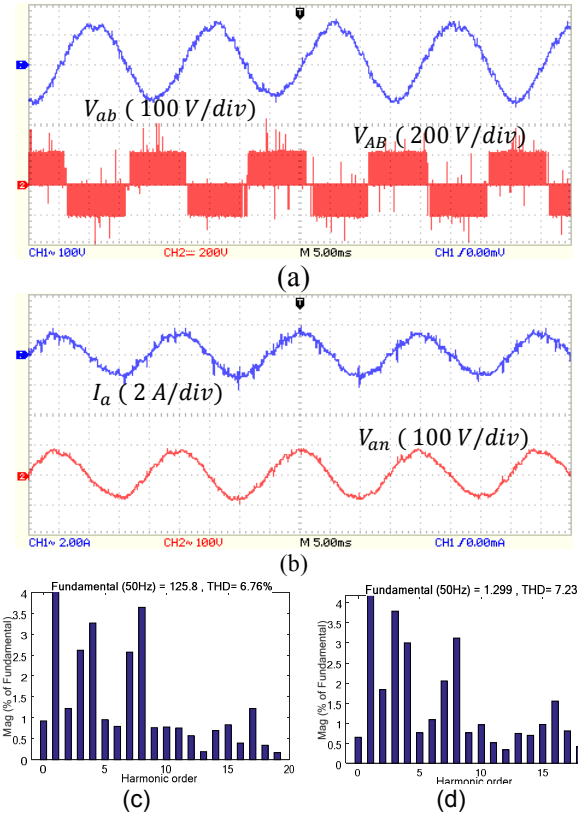


Fig. 15. The experimental results of the proposed topology (SIC-qZSI) with, $V_i = 48V$, $M = 0.8$ and $D = 0.2$. (a) Line-voltage after three phase filter (V_{ab}), and Line-voltage before three phase filter(V_{AB}), (b) load voltage and current(V_{an}, I_a), (c) THD of load voltage, (d) THD of load current.

B. Experimental Results of EB-qZSI

The prototype $EB-qZSI$ is constructed to identify the advantages and disadvantages of the proposed topology ($SIC-qZSI$), and the experimental results are obtained in Figure 16. According to the figure, under the same conditions, the $EB-qZSI$ topology generates a lower voltage than the $SIC-qZSI$ in the DC-link. Therefore, considering the input current, the $SIC-qZSI$ delivers more output power to the load.

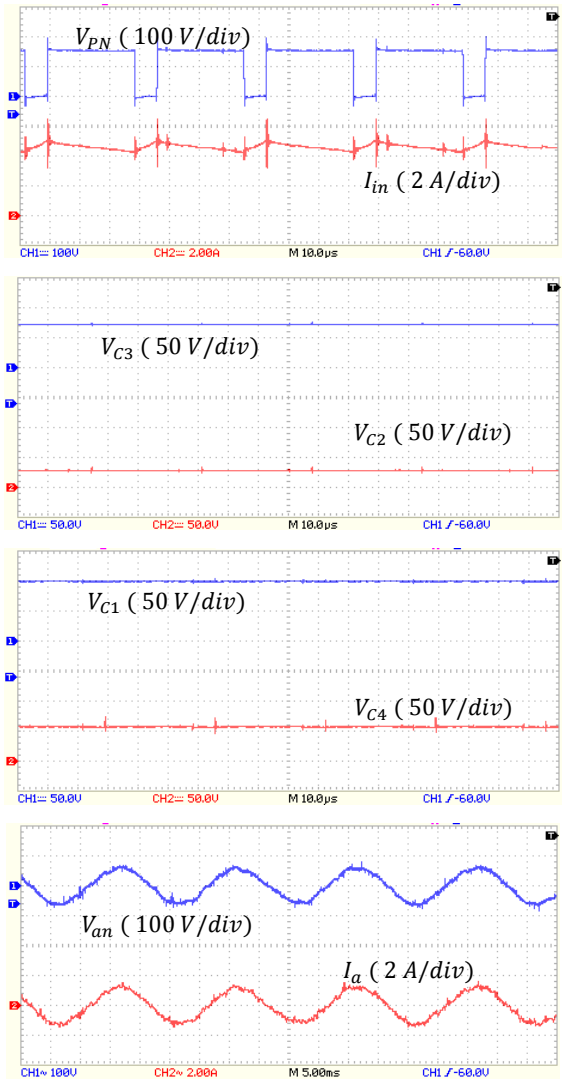


Fig. 16. The experimental results of the EB-qZSI topology with, $D = 0.2$, $M = 0.8$ and $V_i = 48V$. From top to bottom: DC-link voltage (V_{PN}), input current, voltage stresses on capacitors $(C_3, C_2, C_1, C_4$ respectively), voltage and the load current $(V_{bn},\ I_b)$.

C. Power Loss and Efficiency

Fig.17 shows the efficiency at different operating points. These curves have been obtained under different loads in

laboratory conditions with respect to parasitic resistances of Table III. As can be seen, with increasing shoot-through duty cycle (D), efficiency decreases. The proposed topology, due to the lower number of diodes, higher efficiency than the EB-qZSI topology [22], [33].

TABLE III

Parameters of the components for topology proposed and eb-qzsi

Component	Manufacturer	Parasitic Resistance
Inductors	Core: EE, Ferrite Magnetics	$r_L = 0.29\ \Omega$
Capacitors	1000μF/250 V (Nichicon Corp)	$r_C = 0.042\ \Omega$
Diodes	RHRG30120, 30A, 1200V (On Semiconductor) LGU2E102MELB	$r_D = 0.036\ \Omega$
IGBTs	STGW38IH130D, 33A, 1300V (STMicroelectronics)	$r_S = 0.44\ \Omega$

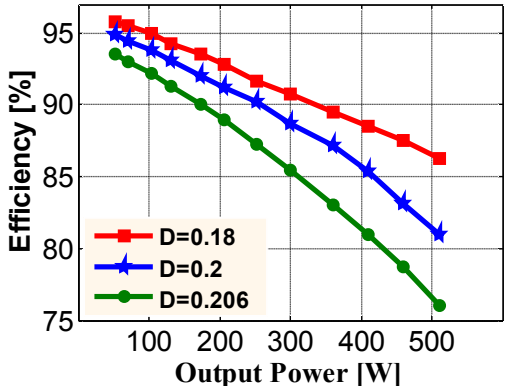


Fig. 17. Measured efficiency at $V_{in} = 80V$ and different operating points

In Fig. 18, the curves of boost factor variations versus the various duty cycles have been compared in the ideal and non-ideal modes. The non-ideal curve of boost factor have been obtained under different duty cycle in laboratory conditions with respect to parasitic resistances of Table III. As can be seen, in the non-ideal state the boost factor increases about 6.3 times at $D = 0.2167$.

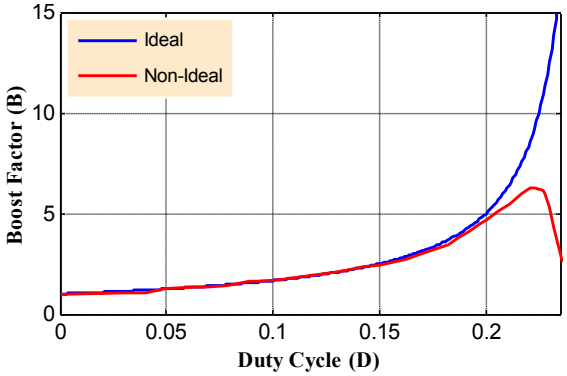


Fig. 18. Plot of boost factor versus duty cycle in the ideal and non-ideal states.

V. CONCLUSIONS

In this paper, a new topology called "switched-inductor/capacitor quasi z-source inverter (SIC-$qZSI$)" from the qZSI family was proposed. This topology, in similar conditions to ESL-qZSI and EB-qZSI topologies, has a higher boost factor and higher voltage gain in the high modulation index and low duty cycle. According to simulation and experimental results, at $D = 0.2167$ has a boost factor of 7.5 and 6.3, respectively. The low voltage stress on the capacitors, the relatively low current ripple, as well as, the higher efficiency due to the fewer diode than other structures were another advantages of this topology. This topology has the characteristics like, current and current ripple equal to all inductors. Also, the voltage stresses on capacitors C_1, C_3, C_4 were equal to their corresponding capacitor's C_2, C_5, and C_6, respectively. Therefore, the proposed topology has a symmetric structure. The experimental results and simulation results were confirmed the relations and performance of the proposed inverter.

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