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A New Multi-Input DC/DC Converter with Coupled and Switched Inductor Applicable for Renewable Energy Sources

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ABSTRACT

To overcome the low output voltage of Renewable Energy Sources (RESs) such as photovoltaic arrays (PVAs) and fuel cells, a new multi-input DC/DC converter is presented in this paper. This converter is based on a combination of modified quadratic buck-boost converters, Switched Inductors (SIs), and Voltage Multiplier Modules (VMMs). The high voltage gain can be achieved by adjusting the duty cycle and turn ratio of the coupled inductor of VMM. This structure inherits all the advantages of the SEPIC converter and using a bidirectional input port (in which an Energy Storage System (ESS) can be connected) and several unidirectional input ports. The load power can be flexibly divided among various power sources. Due to the buck-boost characteristics of the presented converter, it is suitable to charge-discharge the ESS. A Coupled Inductor (CI) is used to couple energy from input to the output equipped with the VMM. Moreover, the use of SI reduces the rise time and ripple of the input current. The stability of the proposed converter against momentary changes of VPV and Ro is the main advantage of this converter. Moreover, considering a secondary ESS as Vi instead of PV allows the converter to be active 24 hours a day. In this converter, the use of two ESSs guarantees the supply of the required output power. In addition, two bidirectional input ports prepare the ESSs charging and discharging capabilities. To verify the analysis and feasibilities of the proposed converter, simulation results are presented

I. Introduction

Increasing demands for energy, air pollution, and depletion of fossil fuels have drawn researcher's attention to renewable energy sources (RESs), such as solar and wind energies. Depending on geographical areas, the power attained from RESs is variable. Therefore, an energy storage system (ESS), as an auxiliary power supply in a multi-input converter (MIC), is required to supply load necessities. The obtained output voltage is relatively low in RESs, such as photovoltaic arrays (PVAs). Therefore, high step-up DC/DC converters (HSUDCs) are widely required to overcome this defect for stepping up DC voltage and supplying inverters and DC loads [1-2]. A family of integrated modules of HSUDCs is reviewed in [3]. In single port converters, each RES requires a separate converter, which needs a different control system. Therefore, this enhances the system's complexity. In multi-port converters (MPCs), different RESs and ESSs are integrated as inputs with one output in a single topology with a simple controller [4]. MPCs can be classified into isolated and non-isolated topologies. Using isolated topologies provides a high gain by using high-turn ratio but with low efficiency and heavy weight [5]. Interleaved and non-interleaved converters are proposed in [6-7] and [8], respectively. In [9-12], a voltage multiplier module (VMM) is added to the converter. In [13-14] the voltage-clamped module (VCM) is added to the converter. Coupled inductors (CIs) and MICs are used in all HSUDCs explored in the following reviews, but ESS besides RES has

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not been considered. In [15-16], VMM and VCM are not considered. A soft-switched three-port converter is presented in [17-18]. There is no auxiliary power supply besides PVA to enhance the converter's ability for supplying a permanent power for output in both presented converters. In [19], because of using multiple CIs and multi-switches in the converter, the efficiency is low. In [20], the high voltage and current stress are the main defects of the converter because the two CIs are directly cascaded. In [21], a two-input DC/DC boost converter based on a coupled inductor and VMM is proposed. The ESS besides RES has not been considered and this is the main defect of this work. In [22], a comparison is made between generalized predictive control and linear controllers in a multi-input DC-DC boost converter, it does not consider ESS besides. Due to the fixed consideration of two inputs in this converter, the PV cannot be used as an input for this converter, which is the main defect of this converter. In [23] a non-isolated single-ended primary-inductor converter (SEPIC)-based multi-input DC/DC converter is presented. This converter inherits step-up/down capability and cannot acts as an HSUDC.

This paper presents a new SEPIC-based multi-input step-up voltage and current converter. The application of switched inductor (SI) instead of input inductance is a good substitute in the proposed converter. Therefore, this substitution minimizes the rise time and input current's ripples. Moreover, this converter has been functionally promoted by applying CI instead of inductor L_2, and adding two VMMs to its output. Therefore, this converter acts as a step-up voltage and current simultaneously, by applying CI with a low turn ratio and two VMMs. Moreover, the stability of the proposed converter against momentary changes of V_{PV} and R_o is the main advantage of the proposed converter. One or more unidirectional port (s) beside one bidirectional port (as a secondary ESS) are considered in this converter as input power sources. Considering a secondary ESS as V_i instead of PV allows the converter to be active 24 hours a day, which is the other important advantage of this converter. This makes the converter to be supplied by various types of RESs.

This paper consists of eight sections. The proposed structure of the converter is presented in Section 2. The proposed converter's functional modes are explained in Section 3. Section 4, explores the converter's power dissipation. Section 5, discusses the proposed converter's dynamic behavior. Section 6, presents a comparison between the proposed converter and other works. The simulation results and power management analysis are presented in the PSCAD environment in Section 7. The last section is devoted to concluding points.

II. Proposed Converter's Structure

Fig. 1 depicts a step-up multi-input SEPIC based on CI, two VMMs, and SI as the proposed converter. The PVA and S_1 are considered the main input and switch of this converter, respectively. The input inductor's structure is a SI based which consists of elements D_1, D_2, D_3, L_{i1}, and L_{i2}. This structure minimizes the input current rise time and ripples. Firstly, the main switch S_1 is turned on, and two inductors L_{i1} and L_{i2} make a parallel structure.

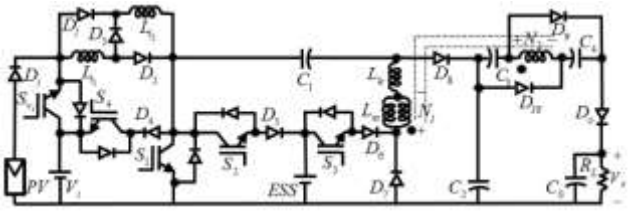

Fig.1. A schematic diagram of the proposed converter

This minimizes the input current's rise time. Secondly, the main switch S_1 is turned off, and two inductors L_{i1} and L_{i2} make a series structure. This minimizes the ripples of the input current after reaching the reference level. The main ESS besides PV is considered for supplying the output power. Switch S_2 and S_3 are applied for charging and discharging the main ESS, respectively. V_i as a secondary ESS is considered for supplying the converter's input power in place of PV at night. Switches S_{vi} and S_4 are applied for discharging and charging V_i, respectively. Magnetic inductor L_m is the output inductor as CI in this converter. In order to raise the load current, the turn ratio is determined low. Moreover, the lesser the CI's turn-ratio determination, the lighter the transformer, the lower the magnetic leakage, and the higher the output current will be attained. By this means, high efficiency can be achieved. Two VMMs are considered to quadruple the secondary voltage of the transformer.

III. Proposed Converter's Functional modes

The demanded output power is assumed constant in this paper. Therefore, three operational modes can be considered by making a comparison between this value and PVA's power. In the first mode, both powers have the same values. This mode is the simplest mode of operation. In this mode, the main switch S_1 is activated. In the second mode, PVA's power is smaller than the output power. This mode consists of two sub-modes, and S_1 and S_3 are triggered. Firstly, only S_1 is activated for reaching the output power to the maximum level attained from PVA. Secondly, S_1 and S_3 are triggered for sending ESS's power to the output for preparing the demanded power. In the 3rd mode, PVA's power is greater than the output demanded power. This mode consists of two sub-modes. Firstly, S_1 is activated so that the output power reaches its desired level. Secondly, the extra power for PVA is transferred through S_2 toward ESS for charging. In the third state of this mode, the extra power of PVA is transferred through D_4 and S_4 after the time ESS is fully

charged to charge the V_i battery. Therefore, V_i can be replaced with V_{pv} by turning on the switch S_{Vi} at night. The other RESs can be added to the input as a replacement of PVA. Therefore, this property makes the converter's input to be expandable. Those aforementioned properties besides the presence of CI, VMMs, and SI produce a converter with a low-ripple and rise-time of input current and step-up voltage/current properties. The following section presents functional modes in detail.

A. The output demanded power is supplied only by PVA (P_{pv}=P_{out})

In this mode, PVA can solely supply the output demanded power, and S_1 is the only switch that is triggered. Figs. 2 and 3 depict two states and time characteristics diagrams, respectively.

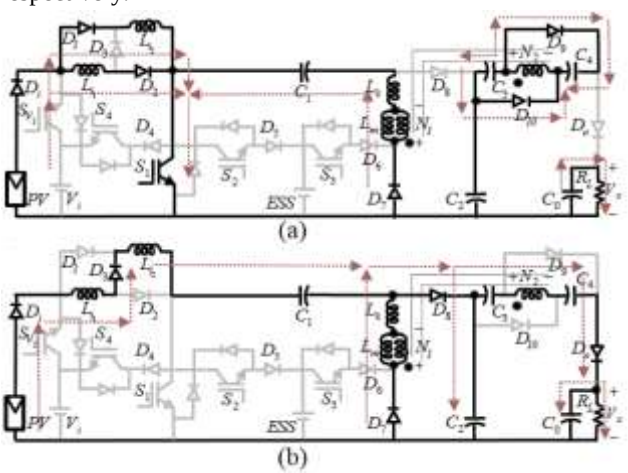

Fig.2. States in the 1st mode; (a): 1st state, S_1 is ON; (b): 2nd state, S_1 is OFF

In accordance with two states (a) and (b) in Fig. 2, (1) and (2) can be derived, respectively. S_1 regulates the inductor current I_{Li}, i.e., the PV's power. Fig. 2 depicts two states as follows.

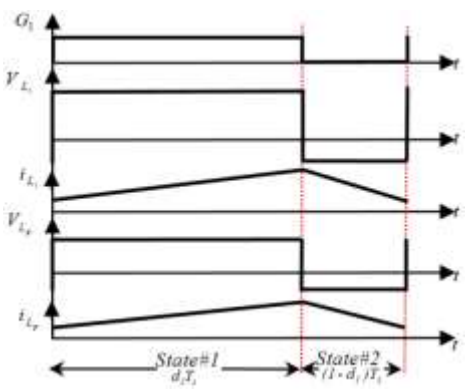

Fig.3. Time characteristic diagrams in the 1st mode

Hint 1:

As Fig. 2 shows, whenever S_1 is turned on, the input inductor L_i is made by a parallel combination of two input inductors L_{i1} and L_{i2}. Therefore, the rise-time of input current goes to a low limit. Whenever S_1 is turned off, L_i is made by a series combination of two input inductors L_{i1} and L_{i2}. Therefore, the input inductor L_i is increased and acts as a high-quality filter for decreasing input current ripples.

a. Switching state1 ($0<t<d_1T_s$)

Fig. 2-(a) shows the current flow in this state. S_1 is turned on, and inductors L_i and L_m are magnetized. Capacitors C_3 and C_4 are charged by the secondary voltage of transformer V_{N2}. V_o is supplied by V_{Co}, and capacitor C_1 is charged by primary voltage V_{N1}. Therefore, (1) can be derived in this state as follows:

$$\begin{aligned} V_{L_i} &= V_{pv}; \\ V_{L_m} &= V_p = KV_1 = KV_{C_1}; \\ V_{C_3} &= V_{C_4} = KNV_{C_1}; \end{aligned} \tag{1}$$

where V_P, K, N, and V_1 are primary voltage, magnetizing coefficient, transformer's turn-ratio, and effective voltage drop in transformer's primary on the 1st state, respectively.

b. Switching state2 (d1Ts <t<Ts)

Fig. 2-(b) shows the current flow. S_1 is turned off, and capacitors C_2 and C_o are charged by the primary and secondary transformers' currents, respectively. Therefore, (2) can be derived in this state.

$$\begin{aligned} V_{L_i} &= V_{pv} - V_{C_1} - V_{C_2}; \\ V_{L_m} &= V_p = KV_2 = -KV_{C_2}; \\ V_{C_3} &= V_{C_4} = \frac{V_o - (1+KN)V_{C_2}}{2}; \end{aligned} \tag{2}$$

where V_2 is the effective voltage drop in the primary on the 2nd state. By applying the volt-second balance equations, (3) and (4) can be deduced as follows:

$$d_1V_{pv} + (1-d_1)(V_{pv} - V_{C_1} - V_{C_2}) = 0;$$

$$V_{pv} - (V_{C_1} + V_{C_2})(1-d_1) = 0 \Rightarrow V_{C_1} + V_{C_2} = \frac{1}{1-d_1}V_{pv} \tag{3}$$

$$d_1V_{C_1} - (1-d_1)V_{C_2} = 0 \Rightarrow V_{C_2} = \frac{d_1}{1-d_1}V_{pv}; V_{C_1} = V_{pv}$$

$$2d_1KNV_{C_1} + (1-d_1)\left[V_o - (1+KN)V_{C_2}\right] = 0;$$

$$\Rightarrow V_o = \frac{d_1(1+KN)}{1-d_1}V_{pv} \tag{4}$$

B. The PV's power is smaller than demanded power (P_{pv}< P_{out})

In this mode, PVA cannot solely supply the output power, and S_1 is triggered so that the output reaches the maximum amount of power that can be supplied by PVA. After this time, S_1 and S_3 are triggered to send ESS's power to output for the power to reach its reference level. This mode can be considered in two sub-modes $d_3>d_1$ and $d_3<d_1$ as follows

where d_3, d_1, S_3, and S_1 are duty cycles, respectively.

I. $d_3>d_1$ in ESS discharging mode

Figs. 4 and 5 depict three states of operation and time characteristics diagrams, respectively.

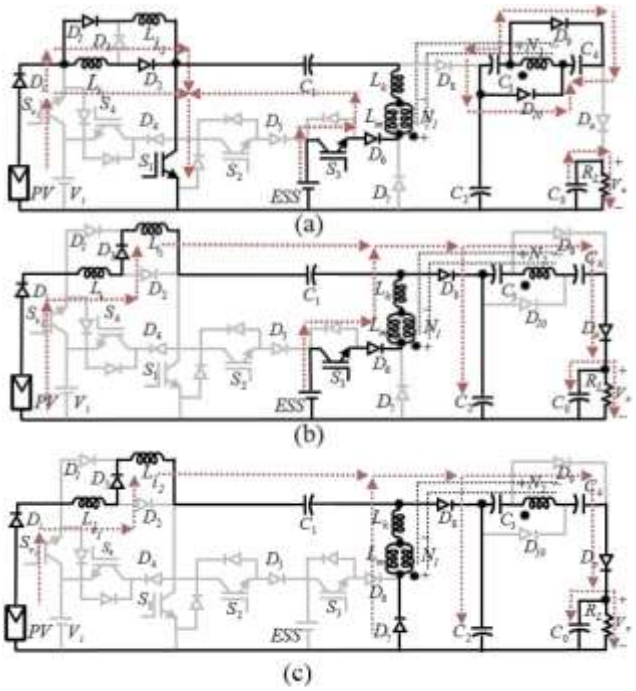

Fig.4. A schematic diagram of the proposed converter in $d_3>d_1$ ESS discharging sub-mode in 2nd mode ($P_{out}> P_{pv}$); (a): 1st state, S_1 and S_3 are ON; (b): 2nd state, S_1 is OFF, but S_3 is still ON; (c): 3rd state, S_1 and S_3 are OFF.

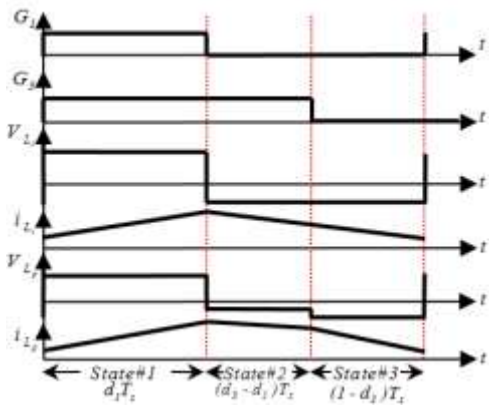

Fig.5. Time characteristic diagrams in $d_3>d_1$ ESS discharging sub-mode in the 2nd mode ($P_{out}> P_{pv}$)

S_1 regulates I_{Li} i.e. PV's power. The discharging rate of ESS is controlled by S_3.

In this sub-mode, three states can be considered as follows:

a. Switching state1 ($0<t<d_1Ts$)

Fig. 4-(a) shows the current flow in this state. S_1 and S_3 are turned on, and inductors L_i and L_m are magnetized. Capacitors C_3 and C_4 are charged by the secondary voltage V_{N2}.V_O is supplied by V_{Co}, and the capacitor C_1 is charged by the primary voltage V_{N1}. Therefore, (5) can be derived.

$$\begin{aligned} V_{L_i} &= V_{pv}\ ; \\ V_{L_m} &= V_p = KV_1 = K(V_{ESS} + V_{C_1}) \\ V_{C_3} &= V_{C_4} = KN(V_{ESS} + V_{C_1})\ ; \end{aligned} \tag{5}$$

b. Switching state2 ($d_1T_s <t<d_3Ts$)

S_1 is turned off, but S_3 is still turned on. Fig. 4-(b) shows the current flow, and capacitors C_2 and C_o are charged by primary and secondary transformer's currents, respectively. Therefore, (6) can be derived.

$$\begin{aligned} V_{L_i} &= V_{pv} - V_{C_1} - V_{C_2}\ ; \\ V_{L_m} &= V_p = KV_2 = K(V_{ESS} - V_{C_2})\ ; \\ V_{C_3} &= V_{C_4} = \frac{V_O - (1+KN)V_{C_2} + KNV_{ESS}}{2}\ ; \end{aligned} \tag{6}$$

Fig. 4-(c) depicts the current flow. S_3 is turned off, and this state and the 2nd state of the previous mode are quite similar. Therefore, (2) can be used in this state. By applying the volt-second balance to (5), (6), and (2) respectively, (7) and (8) can be deduced as follows:

$$\begin{aligned} & d_1V_{pv} + (1-d_1)(V_{pv} - V_{C_1} - V_{C_2}) = 0; \\ & V_{C_1} + V_{C_2} = \frac{1}{1-d_1}V_{pv}; \end{aligned} \tag{7}$$

$$\begin{aligned} & d_1(V_{ESS} + V_{C_1}) + (d_3 - d_1)(V_{ESS} - V_{C_2}) - (1-d_3)V_{C_2} = 0; \\ & d_1(V_{C_1} + V_{C_2}) = V_{C_2} - d_3V_{ESS} \Rightarrow V_{C_1} + V_{C_2} = \frac{V_{C_2} - d_3V_{ESS}}{d_1}\ ; \\ & V_{C_2} = \frac{d_1}{1-d_1}V_{pv} + d_3V_{ESS}\ ; V_{C_1} = V_{pv} - d_3V_{ESS}\ ; \end{aligned} \tag{8}$$

Thus, the output voltage can be attained as (9)

$$2d_1KN(V_{ESS} + V_{C_1}) + (d_3 - d_1)\left[V_0 - (1+KN)V_{C_2} + KNV_{ESS}\right](1-d_3)(V_0 - (1+KN)V_{C_2}) = 0;$$

$$V_0 = \frac{1}{1-d_1}\left\{d_1(1-KN)V_{pv} + \left[d_3(1-d_1) - KNd_1(1-d_3)\right]V_{ESS}\right\};$$

(9) In case $d_3=d_1$, (9) can be simplified as follows:

$$V_O = \frac{d_1(1-KN)}{1-d_1}\left[V_{pv} + (1-d_1)V_{ESS}\right]; \qquad (d_3=d_1)$$

II. $d_3<d_1$ in ESS discharging mode

This sub-mode is just like the previous sub-mode, but the only difference is that $d_3<d_1$. Figs. 6 and 7 depict three states of operation and time characteristics diagrams, respectively.

In this sub-mode, three states exist as follows:

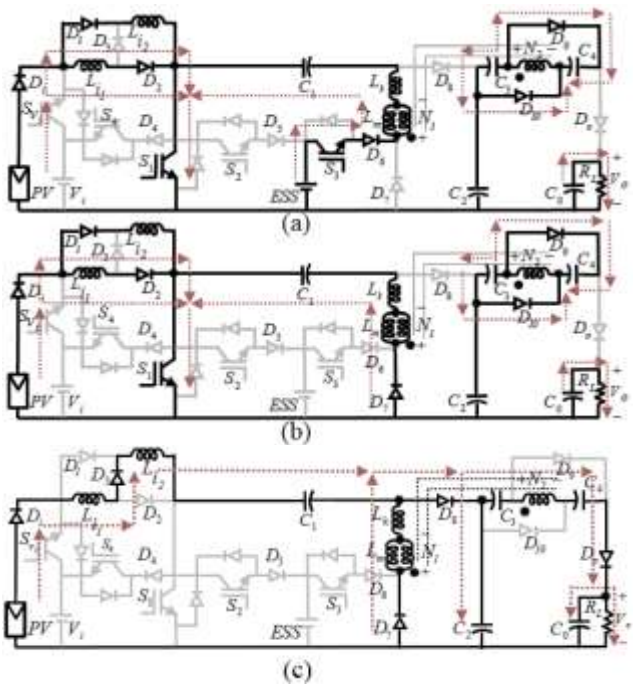

Fig.6. A schematic diagram of the proposed converter in $d_3<d_1$ ESS discharging sub-mode in the 2nd mode ($P_{out}> P_{pv}$); (a): the 1st state, S_1 and S_3 are ON; (b): the 2nd state, S_3 is OFF, but S_1 is still ON; (c): the 3rd state, S_1 and S_3 are OFF.

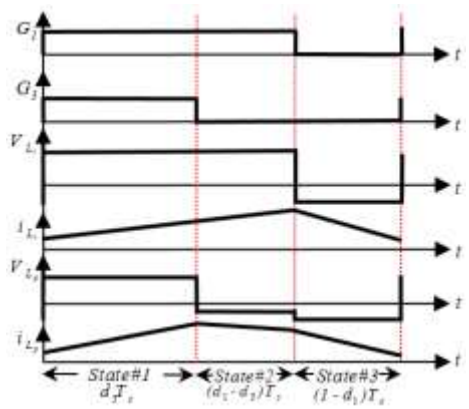

Fig.7. Time characteristic diagrams in $d_3<d_1$ ESS discharging sub-mode in the 2nd mode ($P_{out}> P_{pv}$)

a. Switching state1 ($0<t<d_3T_s$)

Fig. 6-(a) depicts the current flow. S_1 and S_3 are turned on, and this state and the 1st state of the previous sub-mode are quite similar. Therefore, (5) can be used.

b. Switching state2 ($d_3T_s <t<d_1T_s$)

Fig. 6-(b) depicts the current flow. S_3 is turned off, but S_1 is still on. This state and the 1st state of the previous mode are quite similar. Therefore, (1) can be used.

c. Switching state3 ($d_1Ts <t<T_s$)

Fig. 6-(c) depicts the current flow. S_1 is turned off, and this state and the 2nd state of the previous mode are quite similar. Therefore, (2) can be used. By applying the volt-second balance to (5), (1), and (2) respectively, (10) and (11) can be deduced as follows:

$$d_1V_{pv} + (1-d_1)(V_{pv} - V_{C_1} - V_{C_2}) = 0;$$
$$V_{C_1} + V_{C_2} = \frac{1}{1-d_1}V_{pv}; \quad (10)$$

$$d_3(V_{ESS} + V_{C_1}) + (d_1 - d_3)V_{C_1} - (1-d_1)V_{C_2} = 0;$$
$$V_{C_2} = \frac{d_1}{1-d_1}V_{pv} + d_3V_{ESS}; V_{C_1} = V_{pv} - d_3V_{ESS}; \quad (11)$$

Therefore, the output voltage can be attained as (12)

$$2d_3KN(V_{ESS} + V_{C_1}) + 2(d_1 - d_3)KNV_{C_1} + (1-d_1)\left[V_o - (1+KN)V_{C_2}\right] = 0;$$
$$\Rightarrow V_o = \frac{1-KN}{1-d_1}\left[d_1V_{pv} + d_3(1-d_1)V_{ESS}\right]; \quad (12)$$

In the case $d_3=d_1$, (12) can be simplified as follows:

$$V_o = d_1\frac{(1-KN)}{1-d_1}\left[V_{pv} + (1-d_1)V_{ESS}\right]; \quad (d_3=d_1)$$

Hint 2:

From the case $d_3=d_1$ both in (9) and (12), it is clear that by considering a constant amount for d_1 in both case at this point, the output voltages will have equal amounts. As assumed previously, V_o is constant that makes a constant demanded power. Moreover, in conditions which V_{pv} is low, ESS has an important role in supplying the demanded power; Therefore, (12) is applicable for this condition, and (9) can be used whenever V_{pv} is considerably high and it can supply the main amount of the demanded power.

C. The PV's power is greater than demanded power in ESS charging mode.

In this mode, the excess power can be used to charge ESS. This mode can be considered in two sub-modes $P_{pv}>P_{out}$ and $P_{pv}<P_{out}$ as follows

I. $P_{pv}> P_{out}$ in ESS charging mode.

Figs 8 and 9 depict three states of operation and time characteristics diagrams, respectively.

a. Switching state1 ($0<t<d_1T_s$)

Fig. 8-(a) depicts the current flow. S_1 is turned on, and this state and the 1st state of the 1st mode are quite similar. Therefore, (1) can be used in this state

.

b. Switching state2 ($d1Ts <t<(d1+d2)Ts$)

S_1 is turned off and S_2 is turned on. Fig. 8-(b) shows the current flow. The two inductors L_i and L_P (L_m) are demagnetized and their currents flow to ESS for charging. The power transmission occurs through the transformer, and capacitors C_3 and C_4 are charged by V_{N2}. V_o is supplied by

V_{Co}. C_1 is charged by I_{Lm}. (13) can be derived.

$$V_{L_i} = V_{pv} - V_{ESS};$$
$$V_{L_m} = V_p = KV_2 = K(V_{C_1} - V_{ESS});$$
$$V_{C_3} = V_{C_4} = KN(V_{C_1} - V_{ESS});$$ (13)

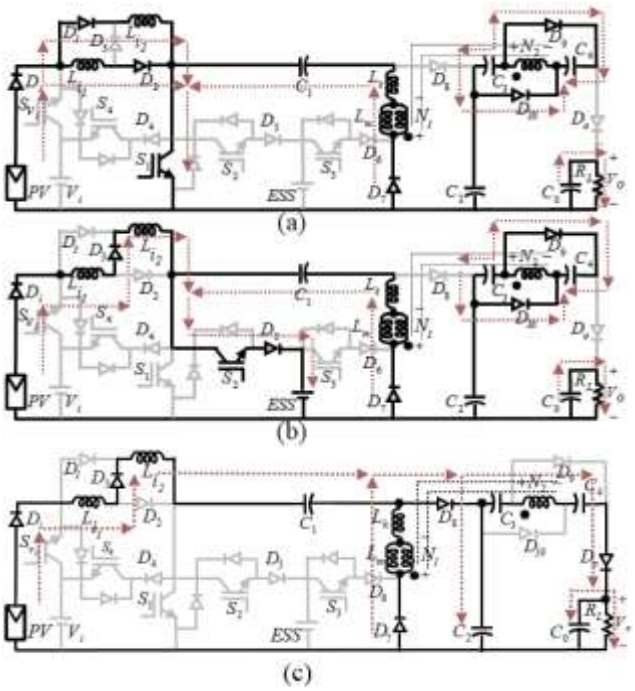

Fig.8. A schematic diagram of the proposed converter in ESS charging sub-mode in the 3rd mode (P_{pv}> P_{out}); (a): the 1st state, S_1 is ON; (b): the 2nd state, S_1 is OFF, but S_2 is ON; (c): the 3rd state, S_1 and S_2 are OFF.

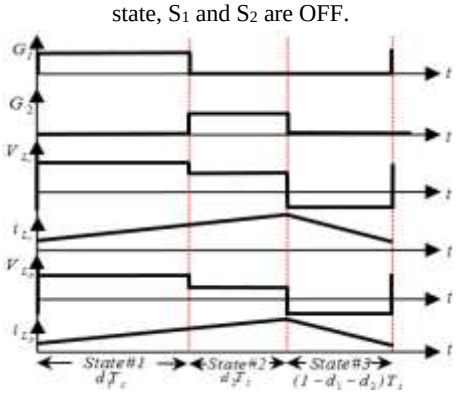

Fig.9. Time characteristic diagrams in the state of P_{PV}> P_{out} in ESS charging states

c. Switching state3 ((d1+d2)Ts <t<Ts)

Fig. 8-(c) depicts current flow. S_1 is turned off, and this state and 2'nd state of 1'st mode are quite similar. Therefore, (2) can be used. By applying the volt-second balance to (1), (13), and (2) respectively, (14) and (15) can be deduced as follows:

$$d_1V_{pv} + d_2(V_{pv} - V_{ESS}) + (1 - d_1 - d_2)(V_{pv} - V_{C_1} - V_{C_2}) = 0;$$
$$V_{C_1} + V_{C_2} = \frac{V_{pv} - d_2V_{ESS}}{1 - d_1 - d_2};$$ (14)

$$d_1V_{C_1} + d_2(V_{C_1} - V_{ESS}) - (1 - d_1 - d_2)V_{C_2} = 0;$$
$$(d_1 + d_2)(V_{C_1} + V_{C_2}) = V_{C_2} + d_2V_{ESS} \Rightarrow V_{C_1} + V_{C_2} = \frac{V_{C_2} + d_2V_{ESS}}{d_1 + d_2};$$ (15)

$$V_{C_2} = \frac{(d_1 + d_2)V_{pv} - d_2V_{ESS}}{1 - d_1 - d_2}; V_{C_1} = V_{pv};$$

Thus, the output voltage can be attained as (16)

$$2d_1KNV_{C_1} + 2d_2KN(V_{C_1} - V_{ESS}) + (1 - d_1 - d_2)\left[V_o - (1+KN)V_{C_2}\right] = 0;$$
$$V_O = \frac{1 - KN}{1 - d_1 - d_2}\left[(d_1+d_2)V_{pv} - d_2V_{ESS}\right];$$ (16)

II. P_{pv}>> P_{out} in ESS charging mode

In this state, the excess power after ESS charging can be used for V_i charging. Fig. 10 depicts three states of operation in the state of P_{pv}>> P_{out} at the time that ESS is fully charged. The excess power is pushed toward V_i for charging by switching on S_4.

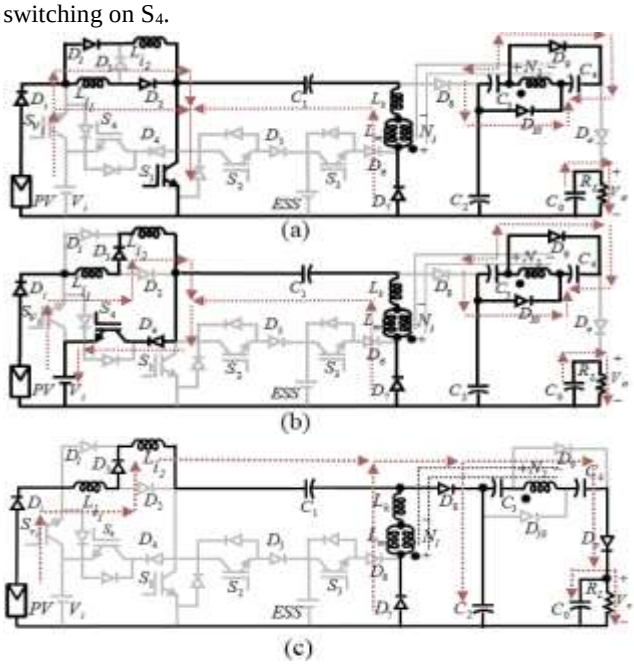

Fig.10. A schematic diagram of the proposed converter in ESS charging sub-mode in the 3rd mode (P_{pv}>> P_{out}); (a): the 1st state, S_1 is ON; (b): the 2nd state, S_1 is OFF, but S_4 is ON; (c): the 3rd state, S_1 and S_4 are OFF.

Hint 3:

In all the above modes, the total input inductor is switched between two quantities. In the first and second steps, two inductors L_{i1} and L_{i2} become parallel and serial with each other, respectively. Therefore, the total input

inductor can be calculated as (17).

$$L_i = d_1 \frac{L_{i_1} \times L_{i_2}}{L_{i_1} + L_{i_2}} + (1 - d_1)(L_{i_1} + L_{i_2}); \quad (17)$$

If $L_{i1}=L_{i2}$ is assumed, (17) will be simplified as (18).

$$L_i = 0.5d_1 \times L_{i_1} + 2(1 - d_1)L_{i_1};$$
$$\Rightarrow L_i = L_{i_1}(2 - 1.5d_1); \quad (18)$$

(18) shows that the total input inductor is related to S_1 duty cycle d_1. Fig.11 depicts L_i amounts by d_1 variations.

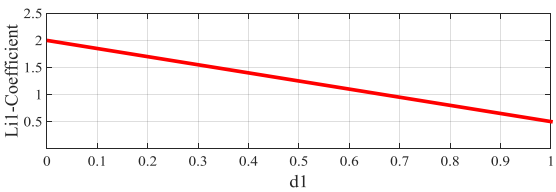

Fig.11. A schematic diagram of the L_{i1} inductor coefficient by d_1 variations (in $L_{i1}=L_{i2}$ assumption)

Hint 4:

As Fig. 11 shows, the first times that d_1 is near one, L_i is on a minimum level which makes a minimum level for the rising time of the input current. As such, the current reaches its desired point in a short time. Then, d_1 approaches the equilibrium point. Therefore, L_i increases and acts as a high quality filter to create minimum ripples for input current.

IV. The converter's power dissipation analysis

The power dissipation of active elements is considered in two groups, the switching and conduction dissipations. The other power dissipation is considered for passive elements as capacitors and inductors [24].

A. *Active elements power dissipation*

a. *Conduction dissipation*

This one is the power that dissipates in elements such as transistors and diodes. This type can be calculated as follows:

$$V_{on,sw}(t)=V_T+R_T I; V_{on,diode}(t)=V_d+R_d I;$$
$$P(t)=V_{on}(t).I(t) \Rightarrow P_{cond,sw}(t)=V_T I+R_T I^2; P_{cond,diode}=V_d I+R_d I^2 \quad (19)$$
$$P_{cond,total} = \frac{1}{T}\int_0^T N_{on,sw}.P_{cond,sw} + N_{on,diode}.P_{cond,diode})dt$$

where, $V_{on, sw}$, $V_{on, diode}$ are the ON-state voltage of the switch and diode, respectively. Moreover, R_T and R_d are the resistance of switch and diode, respectively.

b. *Switching dissipation*

This one is the power that dissipates in switches at the switching times. This type can be calculated as follows:

$$P_{sw} = f_s(N_{on}.E_{on} + N_{off}.E_{off});$$
$$E_{on} = \int_0^{t_{on}} V_{sw}.Idt = \frac{V_{sw}.I.t_{on}}{6}; E_{off} = \int_0^{t_{off}} V_{sw}.Idt = \frac{V_{sw}.I.t_{off}}{6};$$
$$P_{sw} = \frac{f_s.V_{sw}.I}{6}(N_{on}.t_{on} + N_{off}.t_{off}) \quad (20)$$

where, N_{off} and N_{on} are the number of ON-state switches in the current path, respectively. Also, f_s is the fundamental frequency.

Moreover, E_{on} is the energy loss of the switch during the turning-on time and E_{off} is the energy loss during the turning-off time. Moreover, t_{on} and t_{off} are turn-on and turn-off time of the switch, respectively.

Totally, active elements power dissipation can be calculated as follows:

$$P_{active,total} = P_{sw} + P_{cond,total} \quad (21)$$

B. *Passive elements power dissipation*

For inductors and capacitors, a small internal series resistance is considered. These powers can be calculated as below:

$$P_{c,total} = \sum_{i=1}^{8} ESR_i.I_{C_i}^2; P_{l,total} = \sum_{j=1}^{3} R_{l_j}.I_{l_j}^2$$
$$\Rightarrow P_{passive,total} = P_{c,total} + P_{l,total} \quad (22)$$

where, ESR, I_c, I_l, and R_i are equivalent series resistance of capacitors, the current through capacitors, the current through inductors, and internal resistor of inductors, respectively. In this converter, eight capacitors and three inductors are considered.

Therefore, the dissipated power can be calculated as follows:

$$P_{total,dissipated} = P_{passive,total} + P_{active,total} \quad (23)$$

Therefore, the converter's efficiency can be calculated as follows:

$$P_{in} = P_{total,dispated} + P_{out} \Rightarrow 1 = \frac{P_{total,dispated}}{P_{in}} + \frac{P_{out}}{P_{in}};$$
$$\Rightarrow \%\eta = 100\frac{P_{out}}{P_{in}} = 100(1 - \frac{P_{total,dispated}}{P_{in}}) \quad (24)$$

It is important to mention that the power dissipation of the transformer's core is ignored.

C. *Components' design*

The design of components is based on [6] and is considered in the 1st mode of operation. These equations can be written as follows:

$$L_i=\frac{V_{L_i}}{f_s\Delta I_i}=\frac{d_1V_{pv}}{f_s\Delta I_i};V_{S_1-stress}=\frac{V_{pv}-V_{F_{D_1}}}{1-d_1};V_{S_3-stress}=\frac{V_{ESS}-V_{F_{D_3}}}{1-d_3};$$
$$C_o=\frac{I_{Load}}{f_s\Delta V_{c_o}}=\frac{V_{out}}{R_L f_s\Delta V_{out}};V_{S_2-stress}=\frac{V_{pv}-V_{F_{D_1}}-V_{ESS}}{1-d_1-d_2}; \quad (25)$$

Moreover, V_{Lm} can be calculated as below:

$$V_{Lm}=N_p\frac{\Delta BA_e}{(1-d_1)T_s} \quad (26)$$

where ΔB, and Ae, are the magnetic flux density variation and the magnetic core equivalent area, respectively. The turn numbers of the primary and secondary windings can be selected based on the appropriate transformer design guidelines. The apparent power of the HF transformer can be calculated by multiplying the root-mean-square (RMS) voltage and current of the primary winding.

D. The coupled-inductor's transferred power

The power transferred through the coupled-inductor is calculated by multiplying the instantaneous transformer's secondary voltage and current. For this purpose in Figure3, this power can be calculated as follows:

$$at: 0\le t\le d_1T_s \Rightarrow I_{Ls_{in.1'st.state}}=i_{Ls,low}+\frac{i_{Ls,high}-i_{Ls,low}}{d_1T_s};$$
$$at: d_1T_s\le t\le T_s \Rightarrow I_{Ls_{in.2'nd.state}}=i_{Ls,low}-\frac{i_{Ls,high}-i_{Ls,low}}{(1-d_1)T_s};$$
$$I_{Ls}=\frac{I_{Lp}}{N};V_{Ls}=NV_{Lp};P_{transfered.by.CI}=\frac{1}{T_s}\left(\int_0^{d_1T_s}V_{Ls,high}.I_{Ls_{in.1'st.state}}dt\right. \quad (27)$$
$$\left.+\int_{d_1T_s}^{T_s}V_{Ls,low}.I_{Ls_{in.2'nd.state}}dt\right)$$

E. The loss of the elements considerations

For this purpose, a comparison must be done to have an estimation of the dissipation of each group of elements in contrast with the other groups. For this means some assumptions are considered as follows:

1-The power dissipated in each passive element is considered 0.1 watts.

2-The dissipated power of each group of elements is considered approximately the number of element in the converter.

3- The power dissipated in each diode is considered 0.2 watts.

4- The power dissipated in each transistor is considered 1 watt.

Therefore, the portion of each element can be approximately calculated as table1, and its related pie chart is depicted as follows:

TABLE 1
THE POWER DISSIPATED BY EACH ELEMENT

Row	Element	No. of elements presented in a period	Dissipated power of each group (Watts)
1	Inductor	4	0.4
2	Capacitor	4.4	0.44
3	Diode	5.6	1.12
4	Transistor	1	1

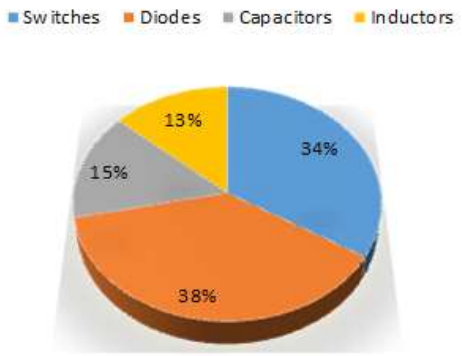

Fig.12. The element's losses pie chart

V. The proposed converter's dynamic behavior

The system's stability around an operating point is described by the system's behaviour in transient state. Primarily, as mentioned in the previous section, the proposed converter operates in four different conditions. In this converter, there will be several inputs and outputs. Therefore, an MIMO control system can be considered for this converter. The state variables are i_{Li}, i_{Lm}, V_{C1}, V_{C2}, and V_{CO}. The state-space average model of the converter can be obtained as follows. In the 1'st operation mode ($P_{pv}=P_{out}$), the average model of the system can be obtained as (28).

$$L_i\frac{di_{L_i}}{dt}=V_{pv}-(1-d_1)(V_{C_1}+V_{C_2});$$
$$L_m\frac{di_{L_m}}{dt}=d_1KV_{C_1}-(1-d_1)KV_{C_2};$$
$$C_1\frac{dV_{C_1}}{dt}=(1-d_1)i_{L_i}-d_1i_{L_m}; \quad (28)$$
$$C_2\frac{dV_{C_2}}{dt}=(1-d_1)\left[i_{L_i}+(1-\frac{1}{N})i_{L_m}\right];$$
$$C_O\frac{dV_{C_o}}{dt}=\frac{(1-d_1)}{N}i_{L_m}-d_1\frac{V_{C_o}}{R_L};$$

In the 1st sub-mode of the 2nd mode (ESS discharging mode ($P_{PV}<P_{out}$, $d_3>d_1$)), the average model of the system can be obtained as (29).

$$
\begin{aligned}
&L_i \frac{di_{L_i}}{dt} = V_{pv} - (1-d_1)(V_{C_1} + V_{C_2});\\
&L_m \frac{di_{L_m}}{dt} = d_1 K(V_{ESS} + V_{C_1}) + (d_3 - d_1)K(V_{ESS} - V_{C_2}) - (1-d_3)KV_{C_2};\\
&C_1 \frac{dV_{C_1}}{dt} = (1-d_1)i_{L_i} - d_1 i_{L_m};\\
&C_2 \frac{dV_{C_2}}{dt} = (1-d_1)\left[i_{L_i} + (1-\frac{1}{N})i_{L_m}\right];\\
&C_o \frac{dV_{C_o}}{dt} = \frac{(1-d_1)}{N} i_{L_m} - d_1 \frac{V_{C_o}}{R_L};
\end{aligned}
\tag{29}
$$

In the 2nd sub-mode of the 2nd mode (ESS discharging mode ($P_{PV}<P_{out}$, $d_3<d_1$)), the average model of the system can be obtained as (30).

$$
\begin{aligned}
&L_i \frac{di_{L_i}}{dt} = V_{pv} - (1-d_1)(V_{C_1} + V_{C_2});\\
&L_m \frac{di_{L_m}}{dt} = Kd_3(V_{ESS} + V_{C_1}) + K(d_1 - d_3)V_{C_1} - K(1-d_1)V_{C_2};\\
&C_1 \frac{dV_{C_1}}{dt} = (1-d_1)i_{L_i} - d_1 i_{L_m};\\
&C_2 \frac{dV_{C_2}}{dt} = (1-d_1)\left[i_{L_i} + (1-\frac{1}{N})i_{L_m}\right];\\
&C_O \frac{dV_{C_o}}{dt} = \frac{(1-d_1)}{N} i_{L_m} - d_1 \frac{V_{C_o}}{R_L};
\end{aligned}
\tag{30}
$$

$$
\begin{aligned}
&L_i \frac{di_{L_i}}{dt} = V_{pv} - d_2 V_{ESS} - (1-d_1-d_2)(V_{C_1} + V_{C_2});\\
&L_m \frac{di_{L_m}}{dt} = Kd_2 V_{ESS} + K(d_1 + d_2)V_{C_1} - K(1-d_1-d_2)V_{C_2};\\
&C_1 \frac{dV_{C_1}}{dt} = (1-d_1-d_2)i_{L_i} - (d_1+d_2)i_{L_m};\\
&C_2 \frac{dV_{C_2}}{dt} = (1-d_1-d_2)\left[i_{L_i} + (1-\frac{1}{N})i_{L_m}\right];\\
&C_o \frac{dV_{C_o}}{dt} = \frac{(1-d_1-d_2)}{N} i_{L_m} - (d_1+d_2)\frac{V_{C_o}}{R_L};
\end{aligned}
\tag{31}
$$

In the 1st sub-mode of the 3rd mode (ESS discharging mode ($P_{PV}>P_{out}$), the average model of the system can be obtained as (31). The state variables and duty cycles can be divided into two components so-called equilibrium and the perturbation points can be assumed as (32).

$$
\begin{aligned}
&x = \bar{x} + \tilde{x};\\
&d = \bar{d} + \tilde{d};
\end{aligned}
\tag{32}
$$

where x, $\bar{x}$, $\tilde{x}$, d, $\bar{d}$, and $\tilde{d}$ are state variable, state equilibrium, state perturbation, duty cycle, duty cycle equilibrium, and duty cycle perturbation, respectively. The perturbations are much smaller than the equilibrium points. Based on this assumption and substituting (32) into (28), the system's small signal model can be achieved. This model can also be represented in matrix form as (33).

$$
\begin{aligned}
&\dot{\tilde{x}} = A\tilde{x} + B\tilde{u};\\
&\tilde{y} = C\tilde{x} + D\tilde{u};
\end{aligned}
\tag{33}
$$

The system's small signal model in operation modes can be expressed as follows:

In the 1st operation mode ($P_{pv}=P_{out}$). (See (34) and (35)).

$$
A = \begin{pmatrix}
0 & 0 & -(1-\bar{d}_1)/L_i & -(1-\bar{d}_1)/L_i & 0\\
0 & 0 & \bar{d}_1/L_m & -K(1-\bar{d}_1)/L_m & 0\\
(1-\bar{d}_1)/C_1 & -\bar{d}_1/C_1 & 0 & 0 & 0\\
(1-\bar{d}_1)/C_2 & (1-\bar{d}_1)(N-1)/NC_2 & 0 & 0 & 0\\
0 & (1-\bar{d}_1)/NC_o & 0 & 0 & -\bar{d}_1/R_L C_o
\end{pmatrix};
B = \begin{pmatrix}
(\bar{V}_{C_1}+\bar{V}_{C_2})/L_i\\
K(\bar{V}_{C_1}+\bar{V}_{C_2})/L_m\\
-(\bar{i}_{L_i}+\bar{i}_{L_m})/C_1\\
\left[(1-N)\bar{i}_{L_m} - N\bar{i}_{L_i}\right]/NC_2\\
-(R_L\bar{i}_{L_m}+N\bar{V}_{Co})/R_L NC_o
\end{pmatrix}
\tag{34}
$$

$$
y = \begin{pmatrix}
\tilde{i}_{pv}\\
\tilde{i}_{ESS}\\
V_{ESS}\\
V_{C_o}
\end{pmatrix};
C = \begin{pmatrix}
1 & 0 & 0 & 0 & 0\\
1 & 1 & 0 & 0 & 0\\
0 & 0 & 1 & 0 & 0\\
0 & 0 & 0 & 0 & 1
\end{pmatrix};
D = 0;
\tilde{x} = \begin{pmatrix}
\tilde{i}_{L_i}\\
\tilde{i}_{L_m}\\
\tilde{V}_{C_1}\\
\tilde{V}_{C_2}\\
\tilde{V}_{C_o}
\end{pmatrix};
\tilde{u} = \begin{pmatrix}
\tilde{d}_1
\end{pmatrix}
\tag{35}
$$

By substituting (32) into (29) and (30), the system's small signal model can be achieved. In the 1st and the 2nd sub-modes of the 2nd mode (ESS discharging mode ($P_{PV}<P_{out}$, $d_3>d_1$ and $d_3<d_1$)), all matrices except B are the same as the 1st operation mode ($P_{pv}=P_{out}$). In all those modes B and $\tilde{u}$ are presented as (36).

$$
B = \begin{pmatrix}
(\bar{V}_{C_1}+\bar{V}_{C_2})/L_i & 0\\
(\bar{V}_{C_1}+\bar{V}_{C_2})K/L_m & KV_{ESS}/L_m\\
-(\bar{i}_{L_i}+\bar{i}_{L_m})/C_1 & -(\bar{i}_{L_i}+\bar{i}_{L_m})/C_1\\
-\left[N\bar{i}_{L_i}+(N-1)\bar{i}_{L_m}\right]/NC_2 & 0\\
-(R_L\bar{i}_{L_m}+N\bar{V}_{Co})/R_L NC_o & 0
\end{pmatrix};
\tilde{u} = \begin{pmatrix}
\tilde{d}_1\\
\tilde{d}_3
\end{pmatrix}
\tag{36}
$$

By substituting (32) into (31), the system's small signal model can be achieved in the 3'rd operation mode ($P_{pv}>P_{out}$ and $P_{pv}>>P_{out}$) as follows:

$$
A = \begin{pmatrix}
0 & 0 & -(1-\bar{d}_1-\bar{d}_2)/L_i & -(1-\bar{d}_1-\bar{d}_2)/L_i & 0\\
0 & 0 & K(\bar{d}_1+\bar{d}_2)/L_m & -K(1-\bar{d}_1-\bar{d}_2)/L_m & 0\\
(1-\bar{d}_1-\bar{d}_2)/C_1 & -(\bar{d}_1+\bar{d}_2)/C_1 & 0 & 0 & 0\\
(1-\bar{d}_1-\bar{d}_2)/C_2 & (1-\bar{d}_1-\bar{d}_2)(N-1)/NC_2 & 0 & 0 & 0\\
0 & (1-\bar{d}_1-\bar{d}_2)/NC_o & 0 & 0 & -(\bar{d}_1+\bar{d}_2)/R_L C_o
\end{pmatrix}
\tag{37}
$$

$$
B = \begin{pmatrix}
(\bar{V}_{C_1}+\bar{V}_{C_2})/L_i & (\bar{V}_{C_1}+\bar{V}_{C_2}-V_{ESS})/L_i\\
(\bar{V}_{C_1}+\bar{V}_{C_2})K/L_m & (\bar{V}_{C_1}+\bar{V}_{C_2}+V_{ESS})K/L_m\\
-(\bar{i}_{L_i}+\bar{i}_{L_m})/C_1 & -(\bar{i}_{L_i}+\bar{i}_{L_m})/C_1\\
-\left[N\bar{i}_{L_i}+(N-1)\bar{i}_{L_m}\right]/NC_2 & -\left[N\bar{i}_{L_i}+N(-1)\bar{i}_{L_m}\right]/NC_2\\
-(R_L\bar{i}_{L_m}+N\bar{V}_{Co})/R_L NC_o & -(R_L\bar{i}_{L_m}+N\bar{V}_{Co})/R_L NC_o
\end{pmatrix}
\tag{38}
$$

$$y=\begin{pmatrix}\tilde{i}_{pv}\\ \tilde{i}_{ESS}\\ V_{ESS}\\ V_{C_o}\end{pmatrix};\ C=\begin{pmatrix}1&0&0&0&0\\1&1&0&0&0\\0&0&1&0&0\\0&0&0&0&1\end{pmatrix};\ D=0;\ \tilde{x}=\begin{pmatrix}\tilde{i}_{L_1}\\ \tilde{i}_{L_m}\\ V_{C_1}\\ V_{C_2}\\ V_{C_o}\end{pmatrix};\ \tilde{u}=\begin{pmatrix}\tilde{d}_1\\ \tilde{d}_2\end{pmatrix} \quad (39)$$

All elements of the matrix in (34), (36), (37), and (38) are fixed except for L_i which varies with d_1.

By calculating the eigenvalues of each matrix A for all operation modes in accordance with the duty cycles' ranges (0 ~ 1), it can be concluded that the real part of them is negative. Thus, this indicates the stability of the system for all modes of operation. Using the numerical values shown in Table 2, the bode diagrams of the proposed converter are obtained as shown in Figures 13-15. As depicted in all figures, the phase and gain margins of the transfer function indicate the stability of the proposed converter.

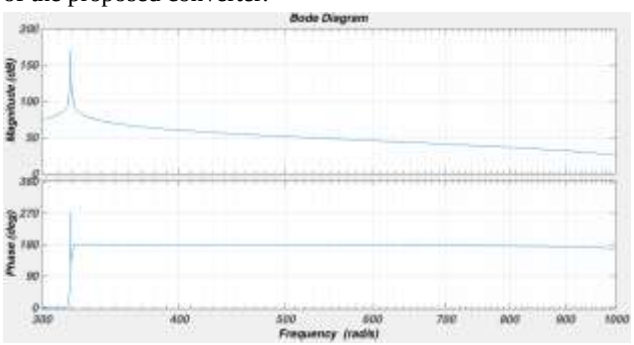

Fig.13. The bode diagram of the transfer function in the 1st mode ($P_{pv}=P_{out}$)

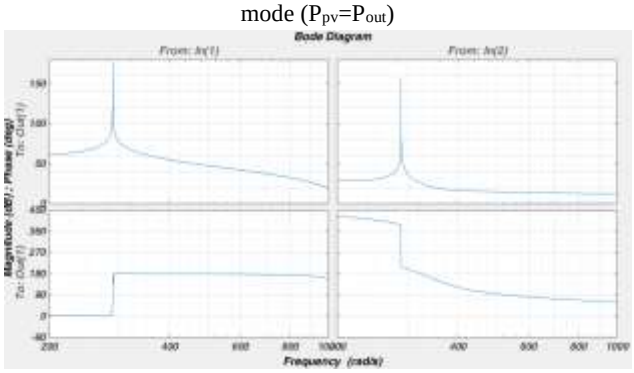

Fig.14. The bode diagram of the transfer function in the 2nd mode ($P_{pv}<P_{out}$)

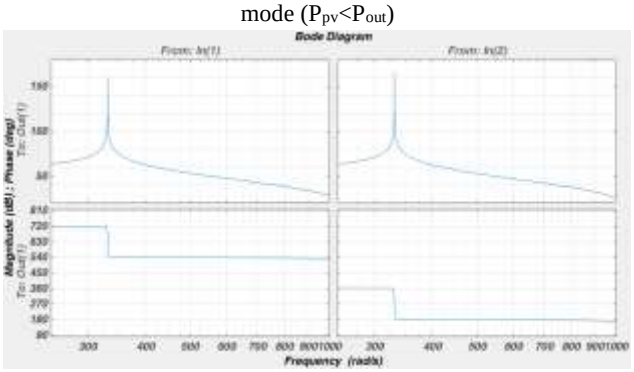

Fig.15. The bode diagram of the transfer function in the 3rd mode ($P_{pv}>P_{out}$)

Fig. 16 depicts the block diagram of a system with its controller. The β and system are the output's feedback coefficient and a controllable plant, respectively.

Fig. 17 depicts the proposed converter with its controller. β is assumed one for all four converters' outputs. This converter has three inputs G_1, G_2, and G_3, which are gate pulses made by the controller for switches S_1, S_2, and S_3, respectively. The outputs i_{pv}, i_{ESS}, V_{ESS}, and V_o are the input current, ESS's charging current, ESS's voltage, and output voltage, respectively.

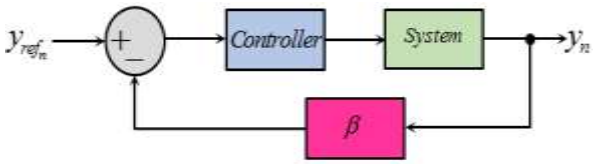

Fig.16. The block diagram of a system with its controller

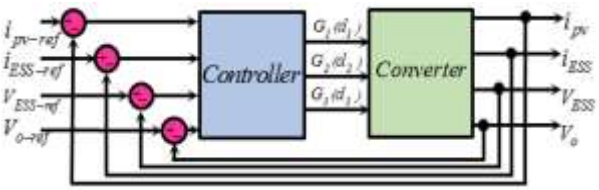

Fig.17. The block diagram of converter with its controller

As Fig. 17 shows, there are four references in accordance with the outputs. The controller makes appropriate duty cycles d_1, d_2, and d_3 for reaching the outputs to desired points.

Fig. 18 shows the designed MIMO block diagram of the controller for the proposed converter. This block has eight inputs consisting of four measured parameters V_o, V_{ESS}, I_{ESS}, P_{pv} and their references. The P_{out} reference is compared to P_{pv}. This comparison decides to set the desired operational mode. The comparators Comp.4 and Comp.5 are considered for this purpose. Comp.1-3 are designated to compare V_o, V_{ESS}, and I_{ESS} with their references, respectively. This controller consists of a number of logic gates, comparators, adders, and a ramp signal generator to generate PWM signals. Because the output of Comp.1-3 must be analogue signals, when implementing the controller, a low-pass filter is placed in the output of these comparators. As such, the integral of their outputs is taken. Therefore, combining a series comparator with a low-pass filter will act like a PI controller .Thus the controller is Logic-PI-PWM-based. The comparators 6-8 are used to convert level to pulse width compared to a ramp signal generator to generate PWM pulses for the three main switches. In order to explain how this controller works, three modes are assumed as follows:

A. $P_{pv}<P_{out}$

The output of Comp.4 is low, but the outputs of gates OR and strobe are high. This allows the pulses generated by comp.6 to appear at the G3 output. Initially, V_o is less than its reference $V_{o\text{-}ref}$, and due to this difference, the output level of

Comp. 1 is non-zero, creating the d_3 duty cycle. Moreover, the output level of Comp. 4 is zero. Therefore, the output of the Min block is zero, and according to the level of difference between V_o and $V_{o\text{-ref}}$, the duty cycle d_1 is generated. A voltage threshold V_t is considered to control the output voltage ripples. When V_o reaches its reference neighborhood, the output of the Max block is zero. This speeds up the controller before it reaches its output reference.

B. $P_{pv}=P_{out}$

All the explanations mentioned in the previous mode apply to this mode except that the strobe output is low. Therefore, G_3 is disabled and G_1 can be triggered.

C. $P_{pv}>P_{out}$

In this case, the output of the strobe is zero. Therefore, the output G_3 is disabled. At first, V_o is lower than its reference value, and the output of Comp. 1 is non-zero. Therefore, the output G_1 is triggered. Whenever, one of or both V_{ESS} and i_{ESS} fall below their (its) reference value(s), the Min will select the minimum value, and the duty cycle d_1 and d_2 are deeply affected by the difference voltage of the output of Comp. 1 and this value. Therefore, the negative result of this subtraction causes outputs G_2 and G_1 to be deactivated and triggered, respectively. Initially, before V_o reaches its reference level, G_1 is the only output that is triggered, after which the G_1 and G_2 will be triggered. The NOT gate is intended to support ESS short circuit.

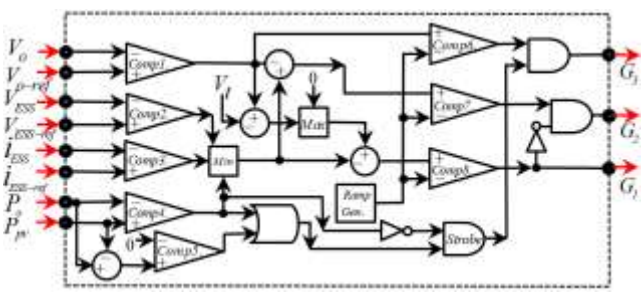

Fig.18. A schematic diagram of the proposed controller

VI. The comparison between the proposed converter and other works

Table 2 presents a comparison between the proposed converter and other works. It shows the three main advantages of this converter over other converters as follows:

1- Regardless of the type of input source used, the proposed converter operates independently and has no dependence on the type of input RES source.

2- The existence of an auxiliary ESS in the proposed converter enables the proposed converter to take over the task of producing power together with the main ESS when it is dark and unable to receive power from the main input. As such, this converter can provide output power 24 hours a day.

3- With the appropriate selection of the winding ratio used in the proposed converter, it is possible to create an increase mode in the output current compared to the input.

4- Due to the increasing property of the output voltages compared to the input in the SEPIC converter and the presence of voltage multipliers in the output of the proposed converter, the voltage gain of the converter reaches a number greater than one. Therefore, according to the third case mentioned above, the proposed converter will have a voltage gain and a current value greater than one at the same time.

5- The presence of the switched inductor in the proposed converter creates a strong filter at the input that reduces the rise time and ripple of the input current.

6- [23], in terms of performance, is the closest converter to the proposed converter. Items 2 to 5 mentioned above are not provided in [23]. The only advantage of [23]'s converter is that it has fewer diodes than our proposed converter (2 fewer). Of course, the proposed converter has 3 more capacitors than [23]'s converter, which is not particularly important due to the lower power losses in the capacitors.

TABLE 2
A PERFORMANCE COMPARISON BETWEEN THE PROPOSED CONVERTER AND THE OTHERS

	Specifications	Structures [6]	[9]	[13]	[23]	Proposed converter
Number of	Coupled Inductor	1	2	1	0	1
	Diode	M+1	4	4	4	6
	Transistor	2	2	1	2	2
	Capacitor	M+2	3	5	2	5
	ESS	0	0	0	1	2
	Bidirectional port	0	0	0	1	2
Stress of	current	Iin1/(1-d2)	IL/d	ILin/d	IL1/d1	ILi/d1
	switch voltage	Vo/n(M+1)	Vo/(2+n)	Vo/(2+n)	(Vpv-VfDi)/(1-d1)	(Vpv-VfDi)/(1-d1)
	Diode voltage	2Vo/n(M+1)	Vo	(n+1)Vo/(n+2)	Vo-VEss	nVLm
RES's Usage		No	No	No	Yes	Yes
RES's type dependence		Yes	Yes	Yes	No	No
Input's expandability		No	No	No	Yes	Yes
Voltage Gain (or Output Voltage)		n(M+1)/(1-d)	(2+n)/(1-d)	(2+n)/(1-2d)	(d1+d3)VEss +d1Vin/(1-d1)	$V_O=\frac{1-KN}{1-d_1}\left[d_1V_{pv}+d_3(1-d_1)V_{ESS}\right]$

where M, n (N), and V_{fDi} are the number of voltage multipliers used in the converter, turn ratio, and forward voltage of diode D_i, respectively.

VII. Simulation results and power management analysis

In this section, the EMTDC/PSCAD simulation results are performed to confirm theoretical analysis of the proposed converter performed here. Figures 18–22 show the simulation results. The values of different elements are summarised in Table 3.

TABLE 3
THE PARAMETERS VALUES

Parameter	Quantity	Parameter	Quantity
C_1	47 µF	L_m	2 mH
C_2	100 µF	Li_1=Li_2	2 mH
C_3	100 µF	L_k	105 µH
C_4	100 µF	V_{pv}	60 ~ 120 V
N	0.5	$V_{ESS-ref}$	24 V
R_L	500 Ω	V_{o-ref}	200V
C_o	220 µF	F_s	40 KHz
C_{pv}	1000 µF	K	0.95

Each mode is presented separately according to Table 4. In this table, the production and consumption power (charge) are marked with a positive and a negative sign, respectively.

The 1st mode: In this mode, only PV is used to supply the output power.

The 2nd mode: In this mode, the power of PV is sent to the output and the excess power is provided by ESS.

TABLE 4
POWER MANAGEMENT IN ALL MODES

Operational Mode No.	Operational Mode	P_{out} (Watts)	P_{pv} (Watts)	P_{ESS} (Watts)	P_{vi} (Watts)
1	$P_{out}=P_{pv}$	-80	+80	Not Used	Not Used
2	$P_{out}>P_{pv}$	-80	+55	+25	Not Used
3-1	$P_{out}<P_{pv}$	-80	+105	-25(ESS Charging)	Not Used
3-2	$P_{out}<<P_{pv}$	-80	+130	-25(ESS Charging)	-20(Vi Charging)

The 3rd mode: In this mode, a part of the power generated by PV, which is requested by the output, is sent to the output, and the excess PV power is spent on ESS charging. To prevent overcharging when ESS is fully charged, the excess PV power will be used to charge. The V_i battery is responsible for supplying power to the input of the converter to generate the output voltage (in the absence of PV at night). The production capacity is marked with a positive sign and the consumption power (charge) is marked with a negative sign.

This converter can be used to supply regional electricity. To change the output load when the household consumption changes, a single-phase inverter is included in the output of this converter in the simulation. The amount of power consumed by the consumer and the power produced by PV can be variable. To consider all the aforementioned situations, the simulation has been done in two states .In the first simulation state, V_{pv} is considered between two levels of 80 and 120 volts. In the second state, these two levels are considered between 60 and 80 volts. In both states, the output load changes between 200 and 400 Ohms (in several moments different from the moments of Vpv changes). Figures 19-21 show the information related to the simulation of the first state and Figures 22-24 also show the information related to the second state.

A. The first state of simulation

As shown in Figure 19, V_{pv} is sometimes changed and at other times, R_o changes between two levels. The output voltage reacts quickly with these changes and reaches the reference level .

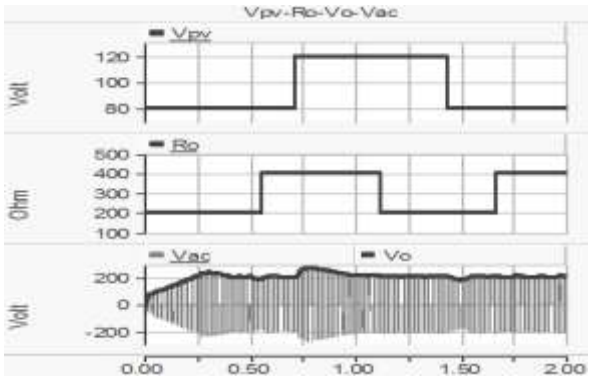

Fig.19 The PSCAD converter simulation results (V_o, V_{ac}, V_{PV}, R_o) in the state of $P_{pv}>=P_{out}$

As shown in figure 20, in the initial times when PV is able to supply the P_{out}, this task is assumed by itself. At times when the output load is low or the power produced by PV is excess, by activating the S_2 switch, this excess power is stored in the ESS.
As shown in this figure, the G_1 gate is only triggered in this mode, and P_{out} is supplied by the P_{pv} alone.

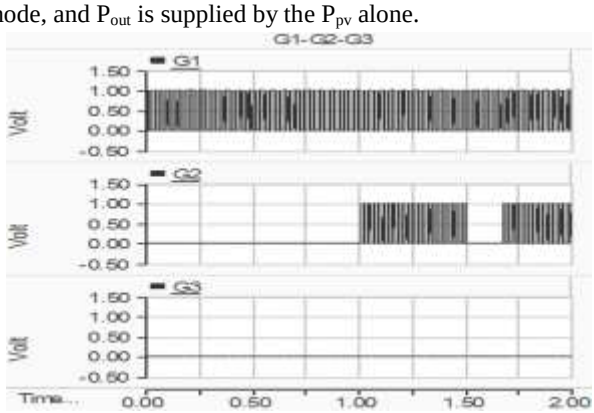

Fig. 20 The PSCAD converter simulation results (G_1, G_2, G_3) in the state of $P_{pv}>=P_{out}$

Figure 21 shows the load current changes according to what is related to V_{ac} in Figure 18. In the same figure, the changes in P_{out} and P_{pv} are shown, which shows that P_{pv} is greater than P_{out}. I_{pv} variations are also specified in this Figure. I_{pv} is associated with a slight overshoot at times when R_o and V_{pv} change, but it appears with a slight ripple in the rest of the times.

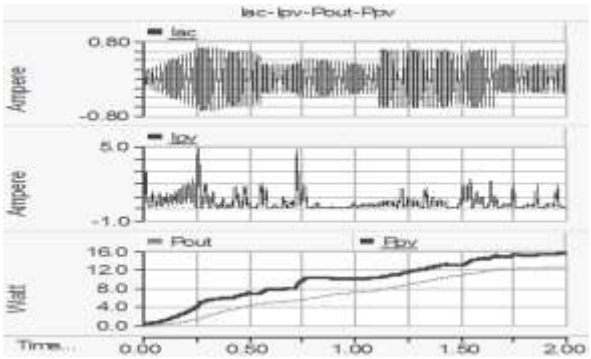

Fig.21 The PSCAD converter simulation results (I_{ac}, I_{pv}, P_{PV}, P_{out}) in the state of $P_{pv}>=P_{out}$

B. Second State of simulation

The output of this state is shown in Figures 22-24. Figure 22 shows the changes in V_{pv} between the levels of 60-80 volts. At different times with these voltage variations, R_o also changes. This figure also shows the outputs of the proposed converter and inverter, which reach the reference level after a short period of time, even with changes in the output load and input voltage. Figure 23 depicts the command pulses of S_1-S_3 switches. When the requested output power exceeds Ppv, switch S_3 is turned on to provide output power with the help of ESS. As it is clear in this figure, S_2 does not work during the entire simulation because there is no excess power for storage.

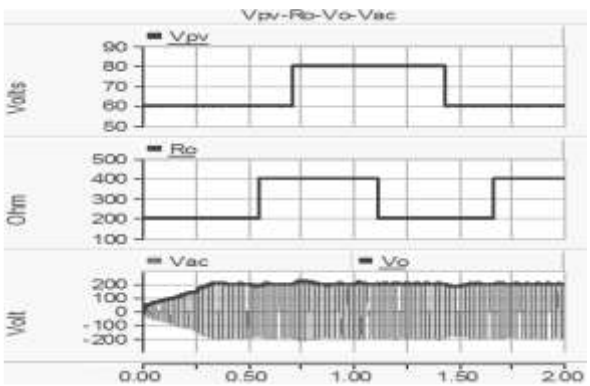

Fig.22 The PSCAD converter simulation results (V_o, V_{ac}, V_{PV}, R_o) in the state of $P_{pv}<=P_{out}$

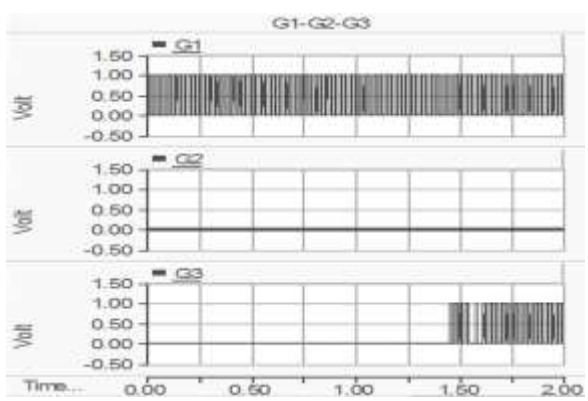

Fig.23 The PSCAD converter simulation results (G_1, G_2, G_3) in the state of $P_{pv}<=P_{out}$

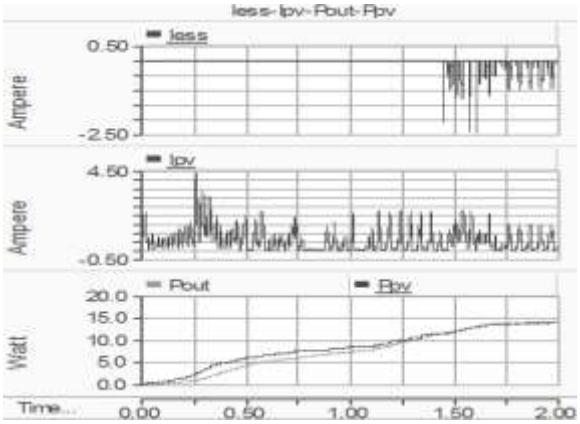

Fig.24 The PSCAD converter simulation results (I_{ess}, I_{pv}, P_{PV}, P_{out}) in the state of $P_{pv}<=P_{out}$

Figure 24 shows the variations in P_{out} and P_{pv} in relation to each other and I_{pv} and I_{ESS} at the time of switching on S_3.

VIII. Conclusions

In this paper, a step-up voltage and current multi-input DC/DC SEPIC-based converter with coupled and switched inductors is proposed. An improved converter has been presented as a novel one by promoting existing structures. The controller strategy based on power management is considered to maximize the use of RES power in this converter. The main advantages of the proposed converter are as follows:

1- The stability of the proposed converter against momentary changes in V_{PV} and R_o. This property is evident according to the simulation results.

2- Considering a secondary ESS as V_i instead of PV allows the converter to be active 24 hours a day.

3- The first priority in providing the power required for the output load is assigned to PV. This means that PV supplies all the load power required; otherwise, it will be done with the help of the main ESS.

4- Due to the use of SI as the input of the converter, the ripple and rise time of the input current is reduced.

5- Due to the use of CI, SEPIC, and VMM, it is possible to simultaneously increase the current and voltage gain.

6- In this converter, it is also possible to use other RES energy sources to supply the input power.

Different modes of operation are discussed and validated via PSCAD simulation results.

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