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# A Cascaded Multilevel Inverter Based on a New Basic Unit

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**ABSTRACT**

In this paper, a new basic unit is proposed for multilevel inverters. Then, a series connection of the proposed basic unit is used to recommend a new topology for multilevel inverters. To determine the magnitude of dc voltage sources, a new algorithm is presented. For the proposed algorithm, different performance parameters such as total voltage rating of switches (TVRS), number of gate drivers, and number of required sources are calculated as a function of the number of output voltage levels and are compared with other topologies. The comparison proves that the proposed cascaded topology requires fewer components and gate driver circuits than most of the other conventional topologies. Moreover, the voltage rating of switches is less than the other topologies which result lower cost and control complexity. Finally, the correctness of the theoretical analysis and the performance of the proposed inverter are verified using the laboratory and simulation results under different scenarios.

## I. Introduction

Among conventional inverters, multilevel inverters have been used for many applications and are one of the most popular solutions in medium and high-power applications [1, 2]. Due to the applicability of multilevel inverters in high-voltage direct current (HVDC), hybrid electrical vehicles (HEV), machine drives, and FACTS devices [3-6], researchers have always suggested ways to optimize their topologies by reducing components, gate driver circuits, and rating of switches [7]. These inverters can produce staircase voltage waveforms with high-quality outputs. The desired output voltage is produced by appropriate switching of several dc voltage sources, which leads to lower rating voltage for switches, less total harmonic distortion (THD), and electromagnetic interference (EMI) [8, 9]. In general, the multilevel inverters are divided into three categories: neutral-point-clamped (NPC) [10], flying capacitor (FC) [11], and cascaded H-bridge (CHB) inverters [12]. The CHB inverters, which are formed by the series connection of basic units, consist of various arrays of power electronic switches and dc voltage sources and are divided into symmetric and asymmetric topologies with equal and non-equal magnitudes of dc voltage sources, respectively. It is important to mention that using non-equal magnitudes reduces the number of required components.

The presented topology in [13] uses non-isolated dc voltage sources with equal amplitudes, and this causes to produce a lower number of voltage levels at the output. Also, the presented structure in [14] needs to a transformer and an H-bridge on the primary side. So, it suffers from high voltage rates on the switches. The presented topologies in [15, 16] utilize a high number of IGBTs and gate driver circuits, and the values of rating voltage on switches are much higher. As a result, the cost and volume of the inverter will be high. The presented topology in [17] can operate in both symmetric and asymmetric conditions. Although, this topology can generate

negative and positive levels at the output and also can reduce the number of switches, but it needs a high number of independent dc voltages sources. To solve this problem, the presented algorithm in [18] can be used. In the presented topologies in [13, 17, 19, 20], the H-bridge is used to generate negative output levels. In [21], two topologies based on developed H-bridge (consists of six switches) are presented. The total standing voltage for these topologies is very high. Although the presented topology in [22] can produce even and odd levels at the output without using H-bridge, but it uses a large number of power electronic elements. The presented structures in [23-28] need to less number of voltage sources, but balancing the voltages across capacitors is the main drawback for these topologies. The presented topologies in [29, 30] need to switches with low voltage rating. So, these topologies are suitable for high-voltage applications, but need to high number of IGBTs and gate driver circuits. The presented topologies in [17, 31] need to bidirectional switches which increase the total cost of inverter.

This paper presents a new topology for multilevel inverters in which the number of power electronic components and rating voltage across the switches are lower. The cascaded multilevel inverter structure is presented in Section 2. Then, a new algorithm to determine the magnitude of the dc voltage sources structure is proposed in Section 3. Section 4 compares the proposed topology with other topologies in terms of the number of IGBTs, rating voltages of switches, and the number of gate drivers. Finally, the laboratory results are presented for the production of a 15-level inverter to prove the feasibility of the proposed topology.

## II. Proposed Cascaded Multilevel Inverter

Fig. 1 shows the topology of the basic unit for the multilevel inverter. This topology consists of eight unidirectional switches, two bidirectional switches with the common-emitter configuration, and three dc voltage sources ($V_1$, $V_2$, and $V_3$). Clearly, the switches ($S_1, S_2$), ($S_3, S_4$), ($S_5, S_6$), ($S_7, S_8$), and ($S_A, S_B$) are fully complementary to have a safe performance and cannot be turned on simultaneously. The switching states of the proposed basic unit to produce different voltage levels are provided in Table 1. In this table, 1 and 0 indicate the on and off states of the switches, respectively. To increase the number of output voltage levels, *n* basic units can be cascaded to form the proposed cascaded multilevel inverter shown in Fig. 2. In this topology, both positive and negative levels at the output are generated. The number of dc voltage sources ($N_{source}$), the number of IGBTs ($N_{IGBT}$) used, and the number of gate drivers ($N_{driver}$) in the proposed cascaded topology can be calculated by the following equations:

$$N_{source} = 3n \quad (1)$$

$$N_{IGBT} = 12n \quad (2)$$

$$N_{driver} = 10n \quad (3)$$

Another important parameter in the cost of inverters is the number of variety voltage sources ($N_{variety}$), which is determined by the variety of the magnitudes of voltage sources. This factor for the topology is calculated by the following equation:

$$N_{variety} = 3n \quad (4)$$

The output voltage of the proposed topology is equal to the sum of the output voltage of all basic topologies. In other words:

$$v_{out} = v_{o,1} + v_{o,2} + v_{o,3} + \cdots + v_{o,n} \quad (5)$$

According to Table 1 and its development for n cascaded units, the maximum output voltage ($v_{o\max,total}$) is obtained as follows:

$$v_{o,total,\max} = \sum_{k=1}^{n}(v_{o,k,\max}) = \sum_{k=1}^{n}(V_{k,1} + V_{k,2} + V_{k,3});\ k = 1,2,3,\ldots,n \quad (6)$$

TVRS is another important parameter in multilevel inverters, which directly affects the price of the inverter. The total rating voltage on the switches of the proposed inverter is as follows:

$$TVRS = TVRS_{us} + TVRS_{bs} \quad (7)$$

where $TVRS_{bs}$ and $TVRS_{us}$ are rating voltage of bidirectional and unidirectional switches, respectively, so that

$$TVRS_{us} = \sum_{k=1}^{n}\sum_{j=1}^{8} V_{S,k,j} \quad (8)$$

where $V_{S,k,j}$ is the value of the rating voltage of the switches $S_{k,1}, S_{k,2}, S_{k,3}, \cdots, S_{k,8}$ of unidirectional switches in the *k*th unit. The rating voltage of unidirectional switches is as follows:

$$V_{S,k,1} = V_{S,k,2} = V_{k,1} \quad (9)$$

$$V_{S,k,3} = V_{S,k,4} = V_{k,1} + V_{k,2} \quad (10)$$

$$V_{S,k,5} = V_{S,k,6} = V_{k,2} + V_{k,3} \quad (11)$$

$$V_{S,k,7} = V_{S,k,8} = V_{k,3} \quad (12)$$

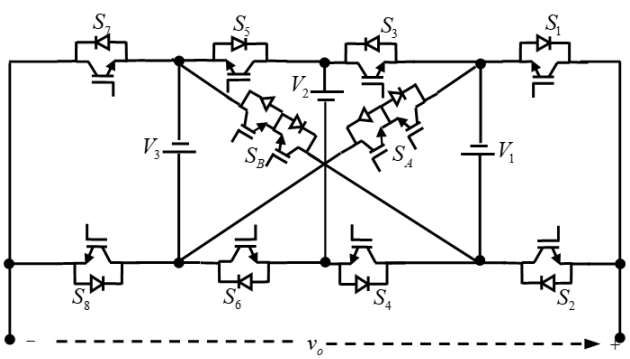



Fig. 1. The structure of the proposed basic unit.

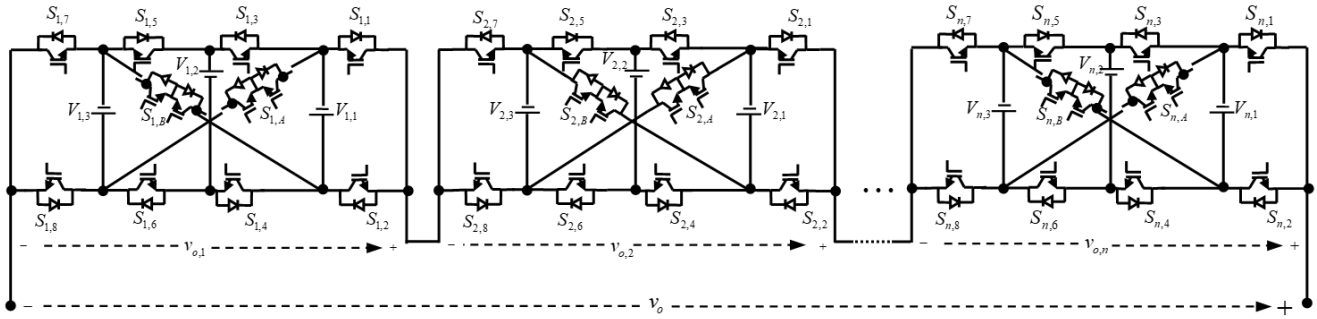



Fig. 2. The proposed cascaded multilevel inverter.

TABLE 1
SWITCHING STATES OF THE PROPOSED BASIC UNIT

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_5$ | $S_6$ | $S_7$ | | $S_8$ | $S_A$ | $S_B$ | $v_o$ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | | 0 | 0 | 0 | $V_1$ |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | | 1 | 0 | 0 | $V_2$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | | 1 | 0 | 0 | $V_1+V_2$ |
| 0 | 1 | 0 | 1 | 0 | 1 | 1 | | 0 | 0 | 0 | $V_3$ |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 | | 0 | 1 | 0 | $V_1+V_3$ |
| 1 | 0 | 1 | 0 | 0 | 1 | 1 | | 0 | 0 | 0 | $V_2+V_3$ |
| 0 | 1 | 1 | 0 | 0 | 1 | 1 | | 0 | 0 | 0 | $V_1+V_2+V_3$ |
| 1 | 0 | 0 | 1 | 0 | 1 | 0 | | 1 | 0 | 0 | $-V_1$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | | 0 | 0 | 0 | $-V_2$ |
| 1 | 0 | 0 | 1 | 1 | 0 | 1 | | 0 | 0 | 0 | $-(V_1+V_2)$ |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | | 1 | 0 | 0 | $-V_3$ |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | | 1 | 0 | 1 | $-(V_1+V_3)$ |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | | 1 | 0 | 0 | $-(V_2+V_3)$ |
| 1 | 0 | 0 | 1 | 1 | 0 | 0 | | 1 | 0 | 0 | $-(V_1+V_2+V_3)$ |

Now, we can calculate $TVRS_{us}$ as follows:

$$TVRS_{us} = 4\sum_{k=1}^{n}(V_{k,1}+V_{k,2}+V_{k,3}) \quad \textbf{(13)}$$

The relation of $TVRS_{bs}$ is given by

$$TVRS_{bs} = (V_{S,k,A}+V_{S,k,B}) \quad (\textbf{14})$$

Considering the following equation:

$$V_{S,k,A} = V_{S,k,B} = V_{k,1}+V_{k,2}+V_{k,3} \quad (\textbf{15})$$

Eq. (14) can be simplified as follows:

$$TVRS_{bs} = 2\sum_{k=1}^{n}(V_{k,1}+V_{k,2}+V_{k,3}) \quad (\textbf{16})$$

Using (6), (13), and (16), the relation of TVRS is obtained as follows:

$$TVRS = 6\sum_{k=1}^{n}(V_{k,1}+V_{k,2}+V_{k,3}) = 6v_{o,toal,\max} \quad (\textbf{17})$$

Determining the magnitudes of dc voltage sources is important to calculate (6) and (17). Therefore, it is necessary to determine the magnitudes of input dc voltage sources for calculating the output voltage and rating voltage on the switches.

## III. Determination of the Magnitude of DC Voltage Sources

Estimating the dc voltage source values is very important for determining the number of output voltage levels. For the proposed topology, it is possible to present different algorithms for determining the magnitude of dc voltage sources. Here, one of them is presented.

In the proposed algorithm, to generate high voltage levels, the following method is proposed to determine the magnitude of dc voltage sources.

**First unit:**

$$V_{1,1} = V_{dc} \quad \textbf{(18)}$$

$$V_{1,2} = 2V_{dc} \quad (19)$$

$$V_{1,3} = 4V_{dc} \quad (20)$$

**Second unit:**

$$V_{2,1} = 2V_{o\max,1}+V_{dc} = 14V_{dc}+V_{dc} = 15V_{dc} \quad \textbf{(21)}$$

$$V_{2,2} = 2V_{2,1} = 30V_{dc} \quad (22)$$

$$V_{3,2} = 4V_{2,1} = 60V_{dc} \quad (23)$$

***n*th unit:**

$$V_{n,1} = 2\sum_{k=1}^{n-1}(V_{o\max,k})+V_{dc} = 15^nV_{dc} \quad \textbf{(24)}$$

$$V_{n,2} = 2V_{n,1} \quad (25)$$

$$V_{n,3} = 4V_{n,1} \quad (26)$$

In this algorithm, the number of output voltage levels, the maximum output voltage ($N_{step,3}$), and the total value of the rating voltage of the switches ($TVRS_3$) are obtained by the following equations:

$$N_{step,3} = 15^n \quad \textbf{(27)}$$

$$V_{out,3,\max} = \frac{(15^n-1)}{2}V_{dc} = \frac{(N_{step,3}-1)}{2}V_{dc} \quad (28)$$

$$TVRS_3 = 3(N_{step,3}-1)V_{dc} \quad (29)$$

## IV. Comparison of Results

This section compares the advantages and disadvantages of the proposed topology with other structures. Fig. 3(a) shows the number of IGBTs against the number of output voltage levels. This comparison confirms the advantage of the proposed multi-level inverter based on the third algorithm due to the use of the least number of IGBTs compared to other topologies. The number of gate drivers against levels in different structures is shown in Fig. 3(b), which indicates that the number of drivers in the recommended structure based on the third algorithm is the same as the topology presented in [16] and it requires a minimum number of drivers compared to other structures. Fig. 3(c) depicts the number of dc voltage sources against the number of output voltage levels. This figure proves that based on the proposed algorithm, the proposed multilevel inverter requires the least number of these sources as compared with the topologies presented in [23, 25, 26, 28], but the topologies presented in [22-25, 28] use capacitors. Considering the importance of rating voltage on the switches, which is one of the most important parameters in determining the cost of multilevel inverters, this parameter is also discussed and compared. Rating voltage of the switches against the number of levels for all three algorithms of the proposed topology has the same relation and does not depend on the magnitude of dc voltage sources.

Fig. 3(d) compares the rating voltage of the switches against the number of levels for the topologies proposed in other references. This comparison indicates that the rating voltage of the switches in the proposed topology is lower than that in the other topologies. Table 2 compares the number of IGBTs, drivers, dc voltage sources, capacitors, diodes, and rating voltage for the switches of different topologies with 69 levels in output voltage and verifies the advantage of the proposed topology. It is worth noting that according to Fig. 1 and Table 1, to generate the output voltage levels, three transistors and one diode or four transistors are instantaneously in the current path. Therefore, the maximum number of components in the current path in the proposed multilevel inverter, is four.

To compare the efficiency of different topologies, it is assumed that all topologies generate 69 levels with the same load and same maximum output voltage. Also, it is assumed that the same switches are used. Under these conditions, based on simulation results, the efficiency of all compared topologies are calculated and summarized in Table 3. According to this table, the efficiency of the proposed topology is better than in comparison to most of the already presented topologies.

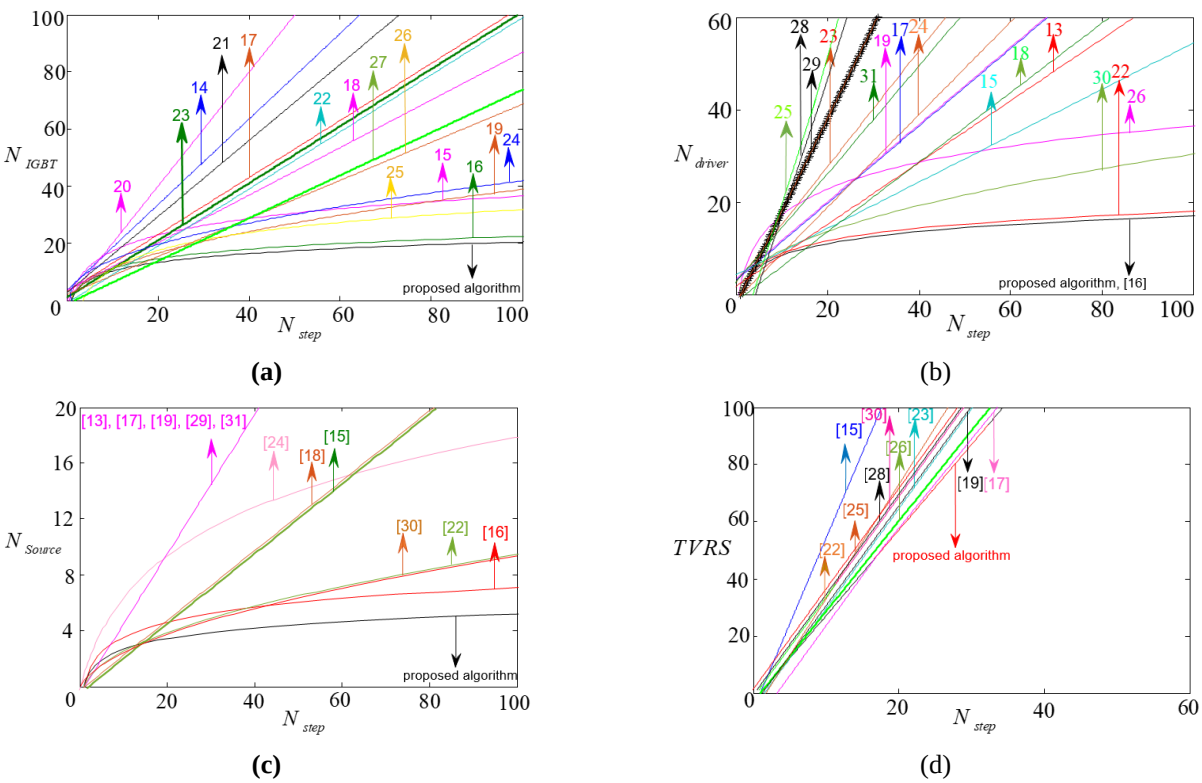



Fig. 3. The results of the comparison: (a) $N_{IGBT}$, (b) $N_{driver}$, (c) $N_{source}$, (d) $TVRS$ versus $N_{step}$.

TABLE 2
THE COMPARISON RESULTS WITH OTHER STRUCTURES FOR PRODUCING 69-LEVEL

| Parameters | $N_{step}$ | $N_{IGBT}$ | $N_{driver}$ | $N_{source}$ | Capacitors | Diodes | *TVRS* |
|---|---|---|---|---|---|---|---|
| [13] | 69 | 61 | 35 | 30 | - | - | - |
| [15] | 69 | 32 | 32 | 11 | - | - | $354V_{dc}$ |
| [16] | 69 | 20 | 15 | 6 | - | - | - |
| [17] | 69 | 63 | 53 | 30 | - | - | $187V_{dc}$ |
| [18] | 69 | 42 | 42 | 11 | - | - | - |
| [19] | 69 | 54 | 54 | 30 | - | - | $206V_{dc}$ |
| [22] | 69 | 22 | 16 | 8 | - | - | $289V_{dc}$ |
| [23] | 69 | 93 | 78 | 1 | 30 | - | $205V_{dc}$ |
| [24] | 69 | 59 | 59 | 15 | 30 | 103 | - |
| [25] | 69 | 170 | 170 | 1 | 34 | - | $236V_{dc}$ |
| [26] | 69 | 27 | 27 | 2 | 4 | 8 | $199V_{dc}$ |
| [28] | 69 | 169 | 169 | 1 | 33 | - | $235V_{dc}$ |
| [29] | 69 | 120 | 118 | 30 | - | - | - |
| [30] | 69 | 30 | 24 | 7 | - | - | $233V_{dc}$ |
| [31] | 69 | 83 | 73 | 30 | - | - | - |
| Proposed Topology | 69 | 18 | 15 | 5 | - | - | $177V_{dc}$ |

TABLE 3
EFFICIENCY COMPARISON

| Parameters | Efficiency [%] |
|---|---|
| [13] | 93.2 |
| [15] | 95.7 |
| [16] | 96.1 |
| [17] | 92.9 |
| [18] | 94.4 |
| [19] | 91.3 |
| [22] | 95.1 |
| [23] | 87.4 |
| [24] | 93.1 |
| [25] | 85.2 |
| [26] | 95.9 |
| [28] | 85.1 |
| [29] | 89.7 |
| [30] | 94.9 |
| [31] | 90.7 |
| Proposed Topology | 94.1 |

## V. Experimental and Simulation Results

In this section, according to Fig. 1, a 15-level inverter with a maximum output voltage of 400V is designed and analyzed. For the simulation and experimental tests, an R–L load with the values of $R$=280.39Ω and $L$=373.1mH is used. The switching frequency is 5kHz, and the minimum error method is used to control the proposed structure. The values of dc voltage sources $V_1$, $V_2$ and $V_3$ are 57, 114, 228V, respectively. Figs. 4 and 5 illustrate the built prototype and experimental results of the output voltage and current waveforms, respectively. Also, the processor AVR ATMEGA 32 was used in the construction of this circuit. Fig. 6 represents the rating voltage on $S_1, S_2, \cdots, S_8, S_A, S_B$ switches with the maximum rating voltage on the switches as 57, 57, 171, 171, 343, 343, 229, 229, 400, and 400V, respectively. The total value of the rating voltage on the switches for the 15-level inverter (the sum of the rating voltage on the switches) is 2400V, which corresponds to Eq. 17. Positive or zero voltages in Fig. 6(a) indicates that the switch $S_1$ is unidirectional and positive, and negative voltages in Fig. 6(i) Fig. 6 shows that the switch $S_A$ is bidirectional.

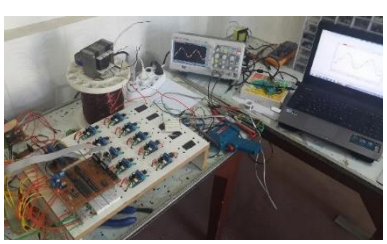
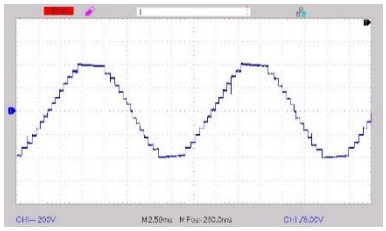
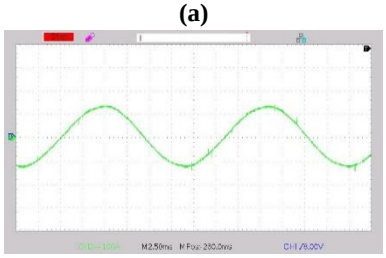


Fig. 4. Laboratory prototype.

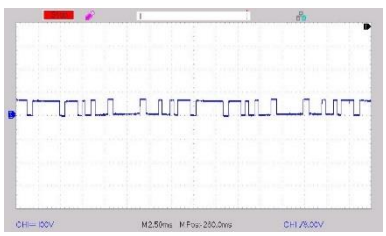


**(a)**

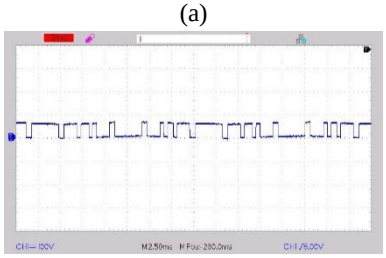


**(b)**

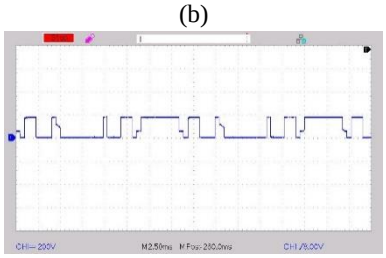
Fig. 5. Experimental results: (a) output 15-level voltage (200 V/div), (b) output 15-level current (1 A/div).



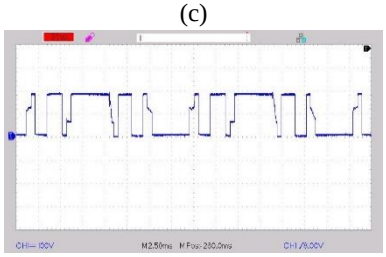
(a)



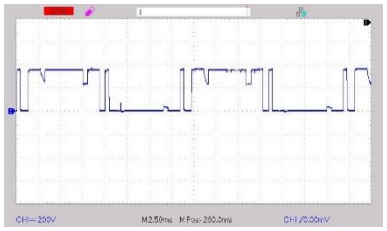
(b)



(c)



(d)



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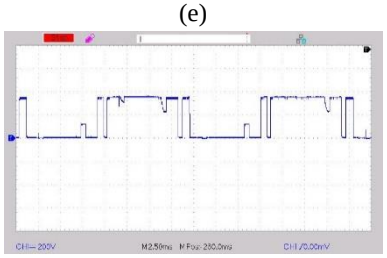
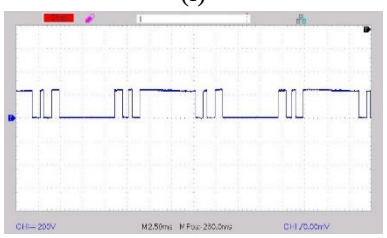
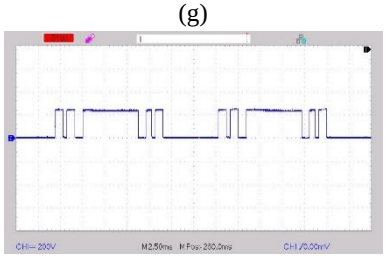


(f)



(g)



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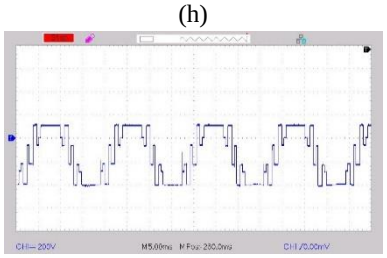
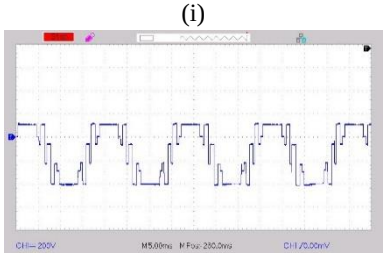


(i)



(j)

Fig. 6. Voltage of switches: (a) S1 (100 V/div), (b) S2 (100 V/div), (c) S3 (200 V/div), (d) S4 (100 V/div), (e) S5 (200 V/div), (f) S6 (200 V/div), (g) S7 (200 V/div), (h) S8 (200 V/div), (i) SA (200 V/div), (j) SB (200 V/div).

To reconfirm the given theories, the simulation results in PSCAD software are given. Fig. 7 shows the simulation results for output voltage and current. Comparing these waveforms with experimental results, shows that there is a good agreement between the simulation and experimental results. Fig. 8 shows the simulation results for switches' current. The maximum value of these waveforms shows the current rating of the switches. It is clear that the current rating of switches depends on the load. By changing the load, these values are changed. Fig. 9 shows the power delivered by each source. To show the correct operation of the proposed topology in different power factors, more simulation results are shown in Fig. 10.

As mentioned before, by series connection of the proposed basic unit, it is possible to generate more levels at the output. For example, by using series connection of two units with the values of dc voltage sources V1, V2, and V3 are 3V, 6V, and 12V, respectively, 225 levels with a maximum output voltage equal to 336V is obtained. The simulation result in PSCAD software for this inverter is shown in Fig. 11.

## VI. Conclusion

This paper presented a new topology for a cascaded multilevel inverter which comprises a cascaded connection of basic units. The proposed topology was analyzed in symmetric and asymmetric modes of operation with the ffundamental frequency switching control method. To highlight the advantages of the proposed topology to the previous topologies, it was compared with a number of other topologies. Based on the results of the comparison, it is found that the proposed cascaded topology has the minimum number of power components, gate driver circuits, and rating voltage on the switches as compared to most of other conventional topologies, resulting in lower cost, volume, and complexity of the control circuits. A 60-level inverter based on the third algorithm proposed technology requires 18 IGBTs and 15 driver circuits and its total rating voltage on the switches is 177V. While to generate the same number of output voltage levels, structures in [23, 17] require 93 and 63 IGBTs and 78 and 53 gate driver circuits, and the total rating voltage on the switches is 205V and 354V respectively. To study the feasibility of the operation of the 15-level inverter based on the third algorithm, experimental results are provided.

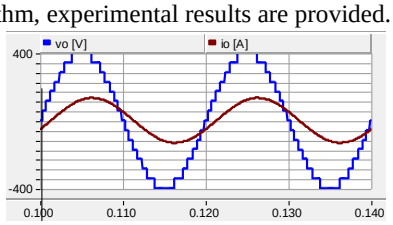



Fig. 7. Simulation results: output voltage and current.

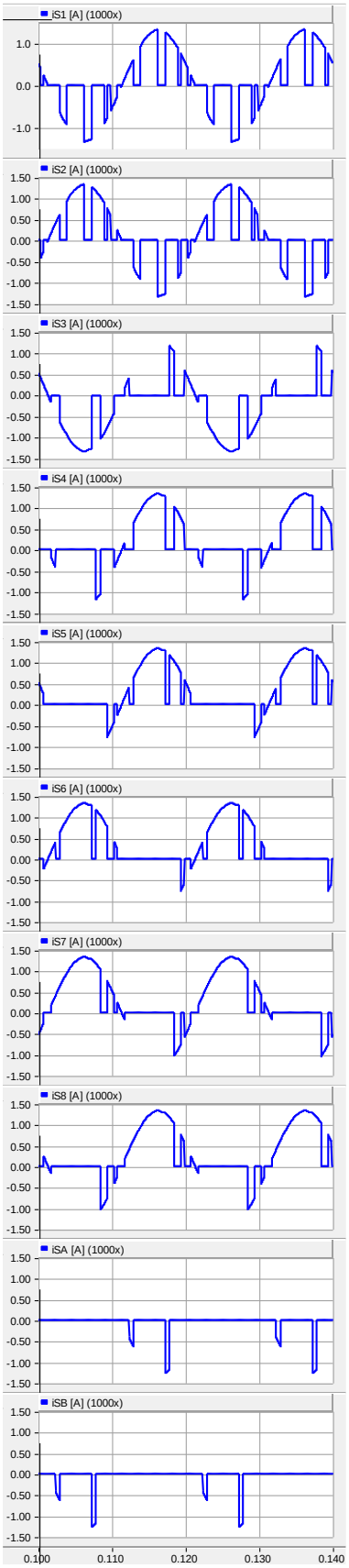



Fig. 8. Simulation results: switches' currents.

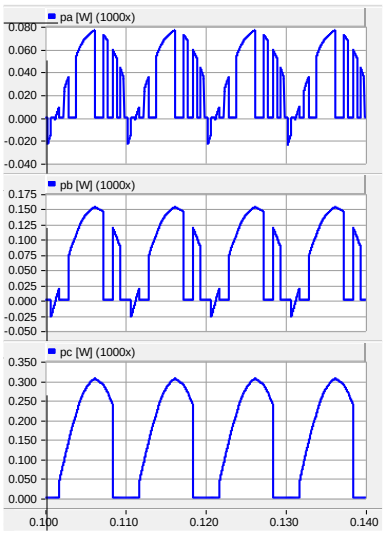
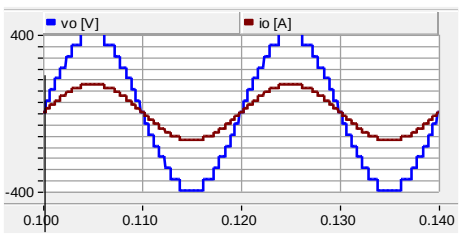
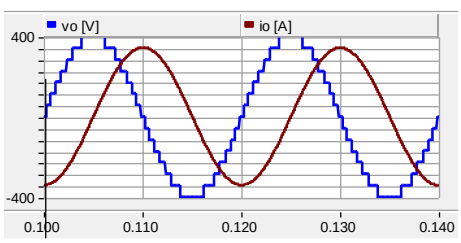


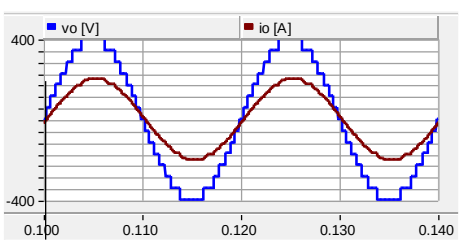

Fig. 9. Power delivered by sources.



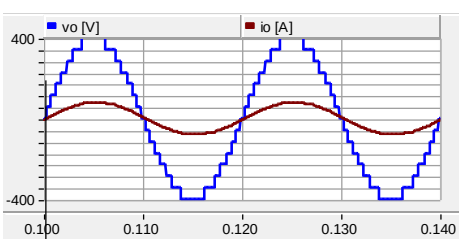

$R$ = 280.39Ω




$L$=373.1$mH$




$R$ = 200Ω, $L$=55$mH$




$R$ = 50Ω, $L$=120$mH$

Fig. 10. Simulation results for different power factors.

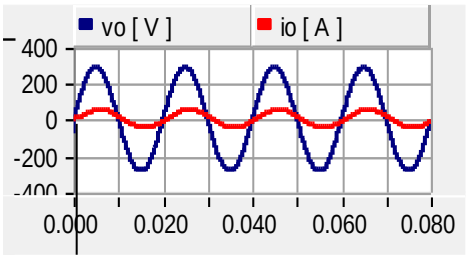



Fig. 11. The output voltage and current waveforms for 225-level cascaded inverter.

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