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Design and Implementation of an N-Type Integer Phase-Locked Loop With Low Phase Noise and Two Output Frequencies at 1 and 4 GHz

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ABSTRACT

This article presents the development and implementation of an integer N-type Phase Locked Loop (PLL) module with two output frequencies of 1 and 4 GHz, each having a loop phase noise better than -110 dBc/Hz@10k. The structure has power levels of 0 and 10dBm at 1 and 4 GHz output frequencies, respectively. Having two different outputs of 1 and 4 GHz at once, in addition to the 1.1 and 4.4 GHz output frequencies realized by the capability included in this design in which two additional outputs can be achieved by using the pins A0 to A4 and altering their status, makes this structure a good candidate for mass production. A two-step frequency division is employed in this work. The first step is realized using the frequency divider of order 4, and the second step is implemented inside the HMC440 IC, including a PFD and a counter so that the output frequency approaches the closest to the reference frequency. Compared to the typical methods, this method presents a clean output by suppressing the spurs meant to be manifested using a single-step frequency division. This PLL is constructed in discrete and modular modes and employed in transceivers' up-converter and down-converter blocks, Satellite communications, Cable TV links (CATV), Local Area Networks (LAN), Global Positioning Systems (GPS), test equipment, digital radios, military and commercial communications. For a specific example, the 4-GHz frequency is used to up-converte or down-converte the received signals, and the 1-GHz frequency is usually used for the synthesizer module clock frequency. Advanced Design System (ADS) software was used in the design of the low-pass filter part of the loop, and OrCAD software was used in the schematic design of the phase lock loop module.

I. Introduction

As long as the Digital Signal Processing (DSP) technology is still incapable of directly processing and generating the Radio Frequency (RF) signals used to transmit wireless data, traditional RF engineering will remain a fundamental part of the design of high-frequency wireless communication systems. Wireless transceivers must still be capable of generating a broad range of frequencies to up-convert the output signal for proper transmission and down-convert the received signal for proper processing. Even though there are various techniques for synthesizing the frequency, using the Phase-Locked Loop wireless communications industry. Like most wireless communication technologies, PLL is relatively new [1]. PLL is a control system with various applications in electronics and communications fields. It contains four basic parts: a Voltage Controlled Oscillator (VCO), a Phase-Frequency Detector (PFD), main and reference dividers, and a loop filter. PLLs can be implemented in two different ways: integer-N and fractional-N.

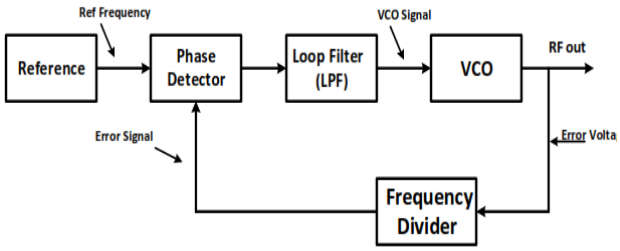

Fig. 1. The conceptual block diagram of a phase-locked loop.

A PLL can produce an output signal, the phase of which is dependent on the input signal. PFD, VCO, and the loop filter are a PLL system's most important and basic building blocks that strongly affect its practicality. In a simple PLL circuit, the reference and the VCO signals are connected to two ports at the input of the PFD circuit. The PFD output, which is an error signal, is applied to the loop filter. Then, the filtered voltage error is fed back to VCO. The diagram of the PLL blocks function is shown in Fig. 1. When the two input signals are small, the PFD block in the PLL circuit is actually a multiplier [2-14].

The two input signals are assumed as

$$v_i(t) = V_s \sin(\omega_i t + \theta_i) \quad (1)$$

$$v_o(t) = V_o \cos(\omega_i t + \theta_o) \quad (2)$$

in which v_i is the input signal applied to PFD, v_o is the PFD's second input from the divider circuit, ω_i is the input signal frequency, θ_i is the input signals phase, and θ_o is the phase of the output signals coming from the divider. The basic loop equation in the diagram shown in Fig. 2 can be achieved as follows:

$$V_d(t) = K_m V_i(t).V_o(t) = \frac{1}{2}K_m V_s V_o \sin(2\omega_i t + \theta_i + \theta_o) + \frac{1}{2}K_m V_s V_o \sin(\theta_i - \theta_o) \quad (3)$$

in which K_m is the multiplying factor in the multiplier with dimensions equal to $[V^{-1}]$. Because of the existence of the low pass filter in the loop, high frequencies can be neglected, and the equation can be rewritten as follows:

$$V_d(t) \approx K_m v_i(t).v_o(t) = \frac{1}{2}K_m V_s V_o \sin(\theta_i - \theta_o) = K_d \sin(\theta_i - \theta_o) \quad (4)$$

in which $K_d = \frac{1}{2}K_m V_s V_o$ is the gain factor of the multiplier in the PFD measured in volts per radian.

According to Fig. 2, the passband of the loop filter can be calculated in the diagram of a PLL system as

$$V_c(s) = v_d(s)F(s) \quad (5)$$

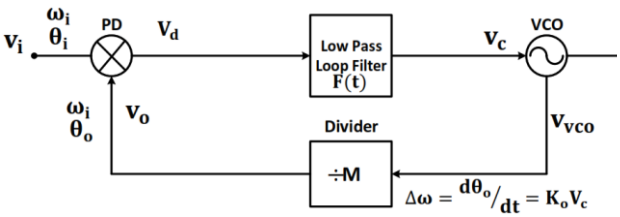

Fig. 2. A PLL diagram with more details.

The phase variations in the VCO circuit are theoretically linear and proportional to the control voltage in the input of the VCO, i.e.,

$$M\frac{d\theta_o}{d_t} = K_o V_c \quad (6)$$

in which K_o depicts the gain factor of the VCO, and M is the dividing order of the divider circuit. Based on the Laplace equations, the basic loop equation can be rewritten as

$$V_d(s) = K_d[\theta_i(s) - \theta_o(s)] \quad (7)$$

$$V_c(s) = v_d(s)\mathrm{F}(s) \quad (8)$$

$$\theta_o = \frac{K_o v_c(s)}{sM} \quad (9)$$

The open-loop transfer function is measured as follows:

$$G(s) = \frac{\theta_o(s)}{\theta_e(s)} = \frac{\theta_o(s)}{\theta_i(s) - \theta_o(s)} = \frac{K_o K_d F(s)}{sM} \quad (10)$$

The phase difference between the two input signals applied to PFD is depicted by θ_e and is measured as

$$\theta_e(s) = \theta_i(s) - \theta_o(s) \quad (11)$$

The closed- loop transfer function of the PLL is achieved as

$$H(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{K_o K_d F(s)}{sM + K_o K_d F(s)} = \frac{G(s)}{1 + G(s)} \quad (12)$$

$$1 - H(s) = \frac{\theta_e(s)}{\theta_i(s)} = \frac{\theta_i(s) - \theta_o(s)}{\theta_i(s)} = \frac{sM}{sM + K_o K_d F(s)} \quad (13)$$

Thus, the input voltage applied to the input of the VCO can be obtained as

$$V_c(s) = V_d(s)F(s) = K_d(s)\theta_e(s)F(s) = \frac{sMK_d F(s)\theta_i(s)}{sM + K_o K_d F(s)} = \frac{sM\theta_i(s)}{K_o}H(s) \quad (14)$$

This Work

This paper presents an integer N-type PLL module with two different output ports, which simultaneously produce two different frequencies of 1 and 4 GHz. The reference frequency of this module is 100 MHz, its bandwidth is 20 KHz, and it is presented as a discrete circuit so that it is implemented by connecting integrated circuits on a board. Based on the requirements, this module possesses two different outputs at the same time according to the required frequency. Also, by designing this module, it becomes possible to achieve two outputs of 1.1GHZ and 4.4GHZ instead of the pre-mentioned outputs by changing the status of pins A0 to A4 in PFD and using the proper VCO, which is suitable for mass production or customer order-based manufacturing of the module. The PCB board is designed with the option of having 4 outputs which are obtainable based on the desirable output between 1, 4 or 1.1, 4.4 GHz. This option is applicable by changing the connection status of the internal counter's pins located inside the PFD chip into voltage or ground and using the proper VCO while mounting the components [15-24].

As the output frequency is considered to be 4 GHz in this PLL, to compare the output frequency with the reference frequency at the input of the PFD, the output frequency must be divided into 40 in a feedback loop by the frequency divider to reach 100 MHz. In the PLL, items like stability, spur cancellation, and phase noise are inevitably important. Thus, for stability, ω_n which is the loop cut-off frequency must be smaller or equal to $0.1\omega_{ref}$ [28].

II. Loop filter

The low pass filter in a PLL block is either passive or active in the second order. H(s) depicts the feedback transfer function, which is, in this case, formed by the divider with the division ratio equal to N = H(s).

The forward transfer function $G_T(s)$ is the loop filter transfer function $G(s) * K_0 * K_d$.

$$Overall\ transfer\ function = \frac{G_T(s)}{1 + G_T(s).H(s)} \quad (15)$$

To obtain a proper control voltage and bandwidth in this module, an active filter is used whose schematics are demonstrated in Fig. 3. To have proper stability, A low frequency zero and pole is used to ensure proper stability. Also, C_2 which is approximately five times smaller than C_1 is used to cancel the reference frequency spurs. Finally, some resistors and some capacitors much smaller than C_1 are added after the filter to cancel all spurs completely.

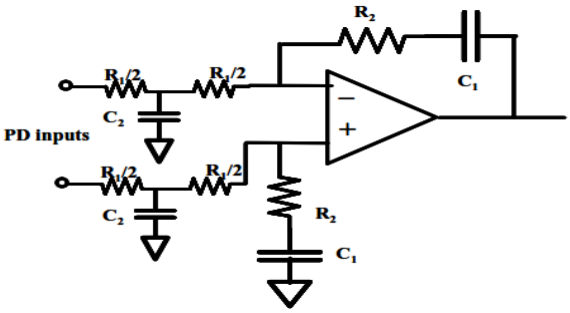

Fig. 3. The active filter structure with OPA211 used in this work.

To obtain a proper control voltage and bandwidth in this module, an active filter is used whose schematics are demonstrated in Fig. 3. To have proper stability, A low frequency zero and pole is used to ensure proper stability. Also, C_2 which is approximately five times smaller than C_1 is used to cancel the reference frequency spurs. Finally, some resistors and some capacitors much smaller than C_1 are added after the filter to cancel all spurs completely. Considering that the number of capacitors added is much lower than C_1, the transfer function is still considered to be of second order with a proper approximation [8, 28-30].

$$\frac{V_o}{V_{in}} = G(s) = \frac{1 + sT2}{(sT1)^2 + 2sT1} \quad (16)$$

The closed-loop PLL [28].

Open-loop gain:

$$LG(s) = \frac{Kd.Ko}{N}.G(s) = \frac{\frac{Kd.Ko}{N}.(1 + sT2)}{(sT1)^2 + 2sT1} \quad (17)$$

Closed-loop gain:

$$H(s) = \frac{\frac{Kd.Ko}{N}.G(s)}{1 + \frac{Kd.Ko}{N}.G(s)} = \frac{1}{1 + \frac{(sT_1)^2 + 2sT_1}{\frac{Kd.Ko}{N}.G(s)(1+sT_2)}} \quad (18)$$

The loop elements are obtained using the characteristics of the VCO, PFD, natural frequency of the loop, division ratio of the loop, and damping factor selected by the designer. These relationships can be expressed in the two following ways.

A) The first method:

Loop filter calculation of R1:

Assumed as Eq. (18)-(24);

$$N = \frac{VCO\ frequency}{Phase\ detector\ frequency} \quad (19)$$

$$\text{Loop bandwidth} = 2\pi.\omega_n \quad (20)$$

$$K_{VCO} = VCO\ sensitivity\ \left(\frac{MHz}{V}\right) \quad (21)$$

TABLE I
RESULTING PHASE MARGINS FROM A GIVEN DAMPING FACTOR

DAMP – FACTOR ξ	Phase Margin (degrees)
0	0
0.5	51.8
0.707	65.5
1	76.3

$$K_{PD} = Phase\ detector\ sensitivity\ \left(\frac{V}{rad}\right) \quad (22)$$

$$\tau_1 = R_1.C_2 \quad (23)$$

$$\omega_n = \sqrt{\frac{K_{VCO}.K_{PD}}{N.\tau_1}} = \sqrt{\frac{K_{VCO}.K_{PD}}{N.R_1.C_2}} \quad (24)$$

Rearrange to get R1 to assume a value for C2;

$$R_1 = \frac{K_V.K_\varphi}{\omega_n^2.N.C_2} \quad (25)$$

Loop filter calculation of R2:
The value of R2 is determined by setting the phase margin of the loop and is related to the damping factor ξ.
The phase margin, which is the difference between the argument of the loop gain and -180° at the frequency where the loop gain becomes unity, is given as

$$\theta = \tan^{-1}\left(\frac{2\xi\omega}{\omega_n}\right) = \tan^{-1}\left[2\xi\sqrt{2\xi^2+\sqrt{4\xi^4+1}}\right] \quad (26)$$

For a range of damping factors, the predicted phase margin can be calculated as shown in Table I [28].

Assuming a damping factor of 0.707 to give us a phase margin of 65°, the value of R2 is given as

$$\xi = \frac{\omega_n.T_2}{2}\ ,\ T_2 = R_2.C_2 \quad \Rightarrow \quad \xi = \frac{\omega_n.R_2.C_2}{2} \quad (27)$$

Loop filter calculation of C1 is obtained as the following assuming that Fc = 10*Fn [28]:

$$\tau_c = \frac{1}{2\pi F_c}\ ;\tau_c = \left(\frac{R_1}{2}\ ||\frac{R_1}{2}\right).c_1\ ;\ \tau_c = \frac{R_1.C_1}{4}$$

$$\Rightarrow \quad C_1 = \frac{4.\tau_c}{R_1} \quad (28)$$

B) The second method:
The above relationships can be summarized to calculate the values of the loop filter elements:

$$C_1 = \frac{k_{VCO}.k_{PD}}{\omega_n^2.N.R_1} \quad (29)$$

$$R_2 = \frac{2\xi}{\omega_n C_1} \quad (30)$$

$$C_2 = \frac{2}{\pi R_1 F_C} \quad ; \quad 10F_N < F_C < F_{PD} \quad (31)$$

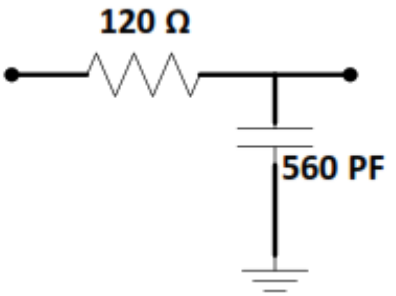

Fig. 4. The low-pass filter with a far pole compared to F_N.

By choosing the value of one of the elements, the values of the other elements of the loop filter are calculated. Since the high-frequency pulses of PFD can cause the nonlinear behavior of the operational amplifier, a low-pass filter is used at the input of the loop filter, and since the structure of the loop filter together with the operational amplifier is an integrator, the input low-pass filter is called a pre-integrator filter that prevents the nonlinear behavior of the operational amplifier by filtering high-frequency pulses.

Generally, the cut-off frequency of the pre-integrator filter is selected at least 10 times the main natural frequency of the circuit so as not to disturb the operation of the main filter. In the above relationships used to calculate the elements of the loop filter, the natural frequency is employed, which is the relationship between the natural frequency of the loop and the F3db bandwidth calculated by choosing ξ. Having known F_{3db}, F_N will be assumed as

$$F_{3db} = F_N\left[1+2\xi^2+\sqrt{1+(1+2\xi^2)^2}\right]^{\frac{1}{2}} \quad (32)$$

Resistance is considered to be $R_1 = 200\Omega$. According to the information included in the information sheet of chips, the parameters of the loop are as follows:

$k_{PD} = 0.3\ \ V/Rad$
$k_{VCO} = 2\pi \times 15\ \ MH/V$
$N = 40$
$F_{3db} = BW = 20\ KHz$
$F_N = 8\ KHz$
$\omega_n = 2\pi \times F_N = 50.24\ KHz$
$\xi = 1$
$C_1 = 10\ nF$
$R_2 = 390\ \Omega$

If $C_2 = 2.7nF$ is selected, the bandwidth of the pre-integrator filter loop will be equal to $F_c = 1.18MHZ$, which is sufficiently larger than $F_N = 8kHz$. Since, in this application, the output frequency of the synthesizer does not change quickly, and there is no high-speed frequency jump, choosing a large value of ξ helps stabilize the loop as much as possible and reduce the unwanted overshoots.

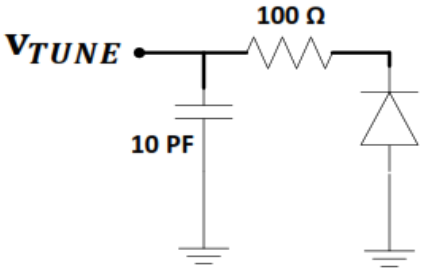

Fig. 5. The internal circuit for the VCO base voltage adjustment.

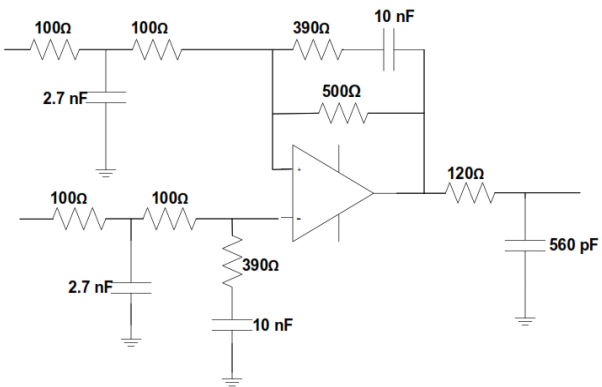

Fig. 6. The final schematic of the loop filter circuit.

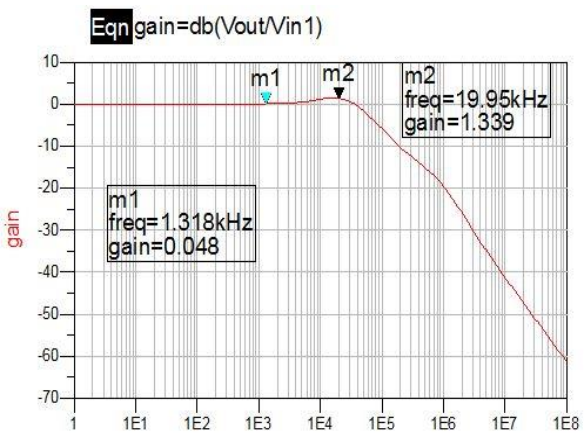

Fig. 7. The frequency response of the simulated active LPF in ADS.

Generally, a low-pass filter with a pole far enough from F_N is used after the main loop filter to prevent the reference signal from settling in the synthesizer output. For this purpose, the circuit of Fig. 4 with $F_{cut} = 2.37\ MHz$ is used.

The important point is that the value of the selected capacitor must be larger enough than the value of the internal capacitor of the next piece, which is actually the VCO so that when these two capacitors are paralleled, the capacitor of the low-pass circuit is dominant.

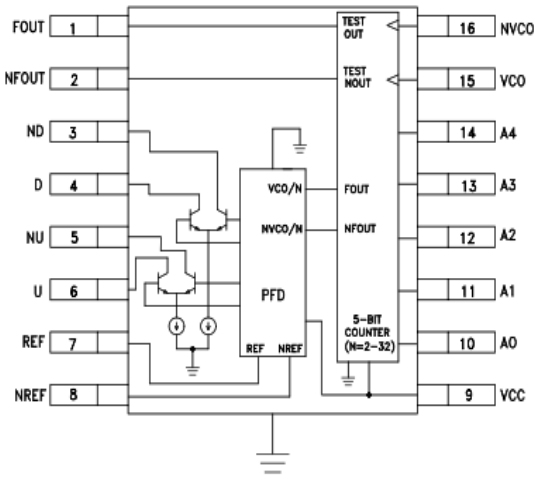

Fig. 8(a).PFD IC internal circuits [35].

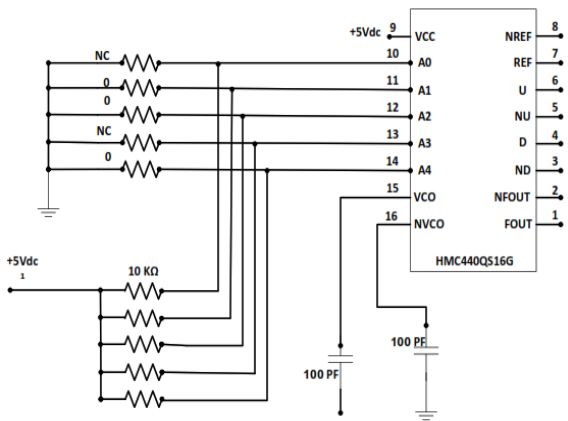

Fig. 8(b).A0-A4 connection.

According to the information sheet of CRO3956A-LF shown in Fig. 5, the base input capacitor of the regulation voltage is equal to 10 pF, as a result of which the value of the low-pass filter capacitor was chosen to be 560pF.

The final phase-locked loop filter is implemented according to Fig. 6. This circuit was first simulated using Agilent Advanced Design System software, and its frequency response is shown in Fig. 7.

III. Frequency divider & pfd

To apply the 4-GHz frequency to the input of the PFD using the feedback loop to be further compared with the reference frequency, the 100-MHz frequency can be achieved by using a frequency divider of order 40. In a single-step frequency division, only one output frequency signal is obtained. Also, a big disadvantage this approach brings to the process is that many spurious tones are created in the single-step division process. In this work, to have two outputs at the same time, the frequency division is realized in two steps, which, in addition to having 2 outputs simultaneously, spurs that were meant to emerge due to the high division order in a single step division are minimized since the frequency division order in the

feedback loop decreases.

In the first step, using the HMC36558GE IC, a frequency divider of order 4, the 4-GHz frequency is divided by 4, thus equaling 1GHz. Given that this frequency divider gives two separate outputs with the same frequency, one is used as one of the two outputs of the PLL with an output frequency of 1 GHZ after amplification.

In the second step, by choosing the order of division using the internal counter within the HMC440 IC, the frequency division circuit is realized by this internal counter, and the order of division is specified by the status of the physical connection of pins A0 to A4 as shown in Fig. 8(b), to ground or voltage. The other 1-GHZ output frequency of the divider mentioned above is, in the first step, divided by 10 and becomes equal to 100 MHz. Then, this 100-MHz frequency is applied to the input of the PFD circuit within the HMC440 IC and compared with the reference frequency. Accordingly, the phase and frequency difference is eventually detected [25-27, 31-34].

IV. PLL design and implementation

Using the technical specifications in datasheet of PFD, OpAmp, VCO, and frequency divider chips and designing the active low-pass filter and according to Equation (33) and all phase noise and loop filter calculator, the product of Peregrine Semiconductor Corporation [46], the estimated phase noise diagram is shown in Fig. 9. The phase noise estimates shown are typical and not exact. Actual phase noise may vary. This value is estimated and obtained according to the calculations from the element datasheet, and it is expected to have worse phase noise after the implementation and measurement. Fvco is the operating frequency of the frequency controller chip with voltage.

According to Figs, 10 and 11, the circuit includes a PLL at 4 GHz, designed for the best achievable phase noise, with the reference input from a 100-MHz OCXO crystal oscillator. The HMC440 chip [36] is used as a PFD in this loop, which has a suitable phase noise. Since the HMC440 chip must bring the output frequency to a value close to the reference frequency in order to compare the output frequency with the reference frequency, the presence of a frequency divider is necessary. For this purpose, a pre-divider by four with chip number HMC365S8G [35] from Analog devices Corporation is used, which consumes less current than similar products of Hittite Microwave Corporation.

As a result to lower current consumption, the total power consumption is lower, thus less heat will be produced.

A VCO with the chip number ROS-3997[37] was also used. It has a good phase noise at 4-GHz frequency. However, it should be noted that there is an expectation that the phase noise measurement results of the implemented module would be worse than the estimated value.

According to the datasheet and calculation[36], the PFD phase noise and the in-loop phase noise are achieved as

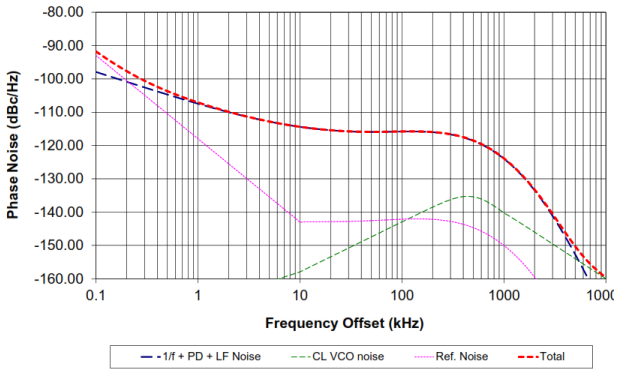

Fig. 9. The PLL phase noise estimated at VCO output (Fvco = 4 GHz; VCO = ZCOMN CRO3956-LF; Ref=Wenzel 100MHz ULN OCXO)

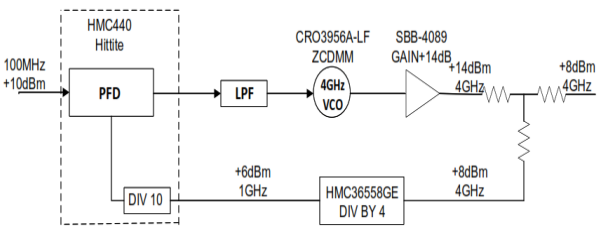

Fig. 10. The proposed PLL block diagram.

$$\text{Phase noise (PFD)} = -153\text{dBc/Hz@10kHz}$$
$$\text{In-Loop Phase Noise} = \text{PFD Noise phase} + 20\log(N) = \text{-121 dBc/Hz @ 10kHz Offset} \quad (33)$$

According to Figs. 11 and 12, the schematics of the PLL module are completed now and simulated using OrCAD.

The output signal of VCO with this structure possesses an output power level of 0 dBm. Then, this output power level is amplified to +14 dBm using an SBB4089 amplifier with a gain equal to +14 dBm. Then, using a resistive power divider, the output frequency is split into two identical branches with frequency and power levels of 4 GHz and +8 dBm, respectively. One of these branches reaches the power level of +10.07 dBm using an SKY65017 [38] amplifier and is reachable using an SMA connector, and the other branch is applied to the frequency divider. On the other hand, the frequency divider used in the feedback loop gives two identical 1-GHz outputs. One is reachable after the required amplification using an SBB4089 [39] amplifier with +1.17 dBm power through an SMA connector. The other output is applied to the input of PFD to be compared to the reference frequency [1, 17, 40-42]. Fig. 13 shows the implemented PLL module and its different building blocks arranged on a board.

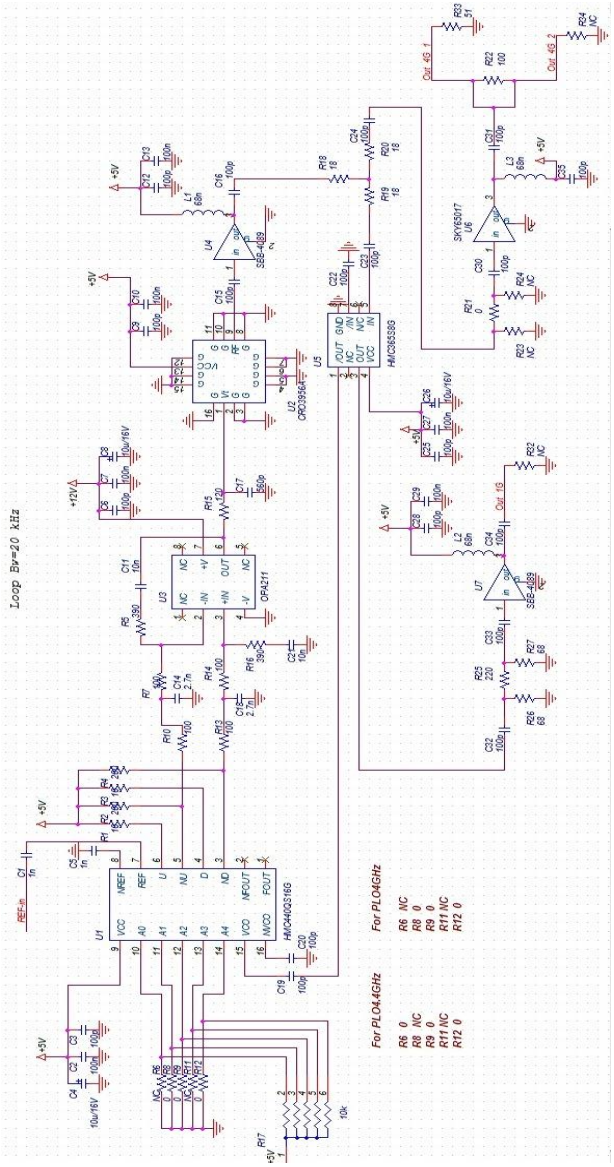

Fig. 11. The completed schematic of the proposed PLL module

Fig. 12. The dimensions of module PLL implemented.

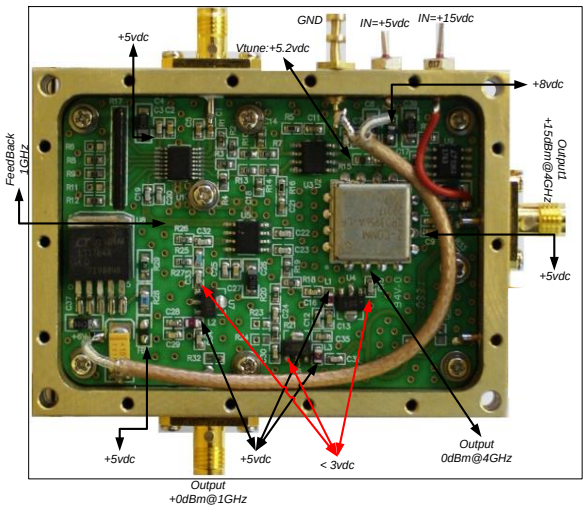

Fig. 13. The final module made with the voltages of the test points.

V. Measurement and results

For testing and commissioning, 15V and 5V power supplies are applied to the module, according to Fig. 13.

Then, a source (i.e., signal generator) gives 100MHz input and 9dBm power to the module, and the module's output is checked in the Spectrum Analyzer. As shown in Figs. 14 and 15, output 1 must have a signal with a frequency of 4GHz with a power of at least 10dBm, and a signal with a frequency of 1GHz with a power of at least 0dBm should be in the output of Output 2. In three span modes, 500 kHz, 10 MHz, and 100 MHz, spur should not be observed in both 4GHz and 1GHz frequencies.

After ensuring the correct operation of the module, the spectrum must be put in Max Hold mode. Then, the module must be put under load for about 12 hours. Spur should not be recorded during this period around the 4GHz signal on the spectrum screen. After the above steps, the following parameters are measured with the spectrum:

1-Signal power

2-Checking spur in three spans: 500 kHz, 10 MHz, and 100 MHz.

3- Phase noise measurement at 10kHz offset

To measure the implemented PLL module parameters, the devices mentioned below were used. The results are explained.

A) Spectrum analyzer Agilent E4407B 9kHz -26.5GHz

B) MXG Analog Signal Generator N5183A 100kHz-20GHz

As can be seen in Figs. 14-17, the measured phase noise and power level in the 4GHz output port are equal to -114.17dBc/Hz and +10.07dBm, respectively, and the phase noise and power level are -117dBc/Hz and 1.17dBm in the 1GHZ output port, respectively.

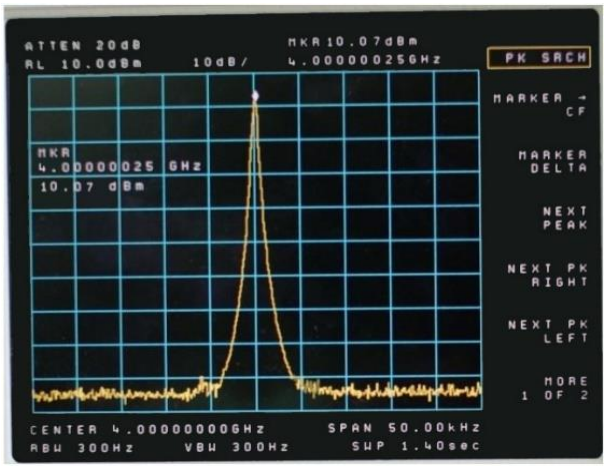

Fig. 14. Measuring the power level of the output port with a frequency of 4 GHz (X-axis= frequency (GHz), Y-axis= power level (dBm)).

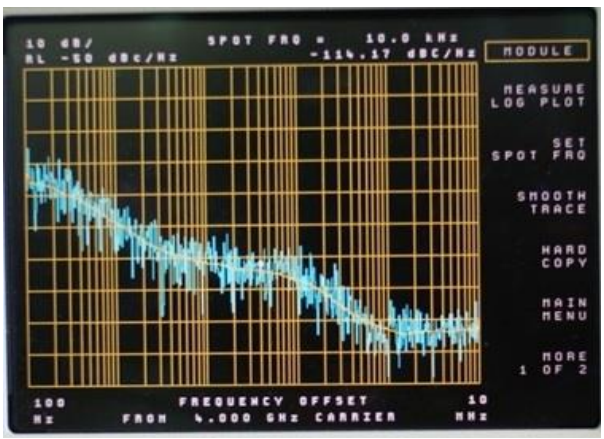

Fig. 15. Output port noise phase measurement with a frequency of 4 GHz (-114.17dBc/Hz @10kHz offset)

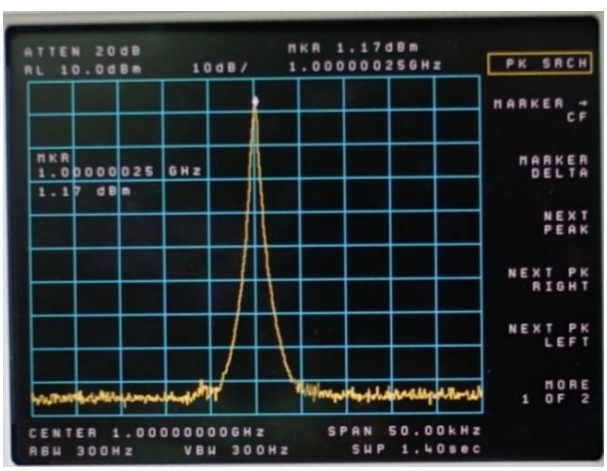

Fig. 16. Measuring the power level of the output port with a frequency of 1 GHz (X-axis= frequency (GHz), Y-axis= power level (dBm)).

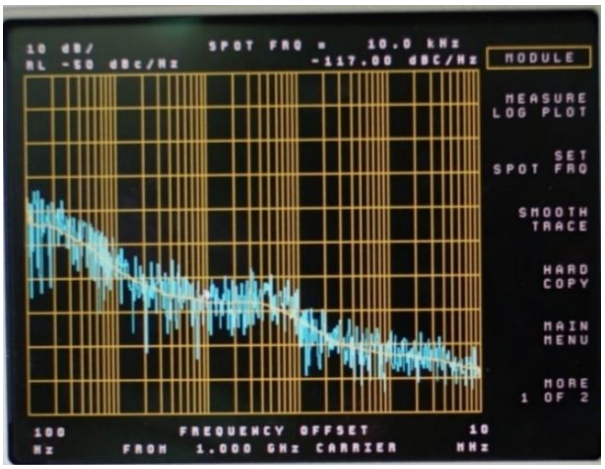

Fig. 17. Output port noise phase measurement with a frequency of 1GHz (-117dBc/Hz @10kHz offset).

The final implemented PLL module with its voltage testing nodes in the circuit is shown in Fig. 13. This module is generally employed in transceiver systems. Detailed experimental results and characteristics of the proposed implemented PLL module are presented in Table II.

According to Table II, this module has two outputs with frequencies of 4 and 1 GHz, each of which has a power level equal to +10.07 and +1.17 dBm, respectively, and a phase noise less than -114 and -117 (dBc@10kHz). The input reference frequency is 100 MHz, and the power level of the input signal is +9 dBm. This module is powered by voltages of +15 and +5 Vdc. It has a current consumption of less than 10 and 1000 mA at the input, respectively. The working temperature of this module is from -40 to +80 ◦C, and it is implemented with the dimensions of 2.91 x 2.12 x 0.39 inches.

Various American companies (including Fairview Microwave [43], Dynamic Microwave [44], Millimeter Wave Products Inc.[47], Raditek Inc.[48], Z-Communication Inc.[49], Lotus Communication systems Inc.[50]) have been active in the field of manufacturing phase-locked modules and have products that can be supplied to customers.

Given that the work presented in this article is discrete (not on-chip), the best comparison would be through comparison with similar products. Therefore, among the products of active companies in this field, a product that is similar to this work in terms of application and frequency range has been selected for comparison, and the results of comparing the technical characteristics of PLL made with similar products have been presented. Table III.

TABLE II
TECHNICAL SPECIFICATION OF THE PLL MOUDULE MADE

Quantity	Description	Specification
Output	Frequency(GHz)	4&1
	Power(dBm)	+10.07 & +1.17
	phase noise (dBc@10kHz)	<-114 & <-117
Reference	Input ref.(MHz)	100
	Input power(dBm)	+9
Electrical	Supply Voltage (Vdc)	+15 & +5
	Input Current (mA)	<10 & <1000
Connector table	15V	Feed Thru
	5V	Feed Thru
	GND	Feed Thru-GND
	REF	SMA-F
Dimension	mm	73 × 53 × 9
Operating temp.	◦C	−40 to +85°C

TABLE III
PERFORMANCE SUMMARY OF THE FOUR PLL

Quantity	This work	[43]	[44]	[45]
PLL Type	INTEGER-N	INTEGER-N	-	INTEGER-N
Output freq. (GHz)	4&1	4	1-50	4 or 5
Out. Power (dBm)	10.07 & 1.17	+7	13-25	-
Phase Noise (dBc/Hz@ 10 KHz)	< -114 & < -117	-110	-110	-111
Rrf Freq. (MHz)	100	100	10 or 5	100
Input power (dBm)	+9	+7	-	+7
Supply Voltage (Vdc)	+15 & +5	+12	+12&+15	2.7
Input Current (mA)	<10 & <1000	150	330	75
Connector	SMA-F	SMA-F	SMA-F	Solder pins
Dimension (mm)	73 × 53 × 9	50.8 × 38.1 × 15.24	57 × 57 × 32	-
Implementation Type	Discrete	Discrete	Discrete	The compact 44-lead (CQFP) PACKAGE
Operating temp.	−40 to +85°C	−30 to +70°C	−55 to +105°C	−40 to +85°C

VI. Conclusions

Design procedures for N-type integer non-integrated modular PLL lead to four different outputs using four external pins. This versatility makes it a good candidate for mass and consumer-based production. The phase noise and the power level of the generated frequency signals are equal to -114.17dBC/Hz and 10.07dBm for the 4GHz output and -117dBC/Hz and 1.17dBm for the 1GHz output, respectively. Compared to the previous works, the designed PLL shows good performance regarding each output's phase noise and power level, as well as power consumption and module size. Also, the low phase noise of the output signals shows that this module is good for the high-precision up/down converting process for K-band signals in K-band transceivers.

VII. Acknowledgment

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