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A Single Switch Transformer-Less DC-DC Converter with Continuous Input Current for Photovoltaic Applications

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ABSTRACT

In this paper, a single switch transformer-less DC-DC converter with continuous input current for photovoltaic applications is proposed. The suggested configuration utilizes a $CL^1C^2D^2$ structure to achieve a high voltage gain and alleviate voltage stress on the semiconductor components. The voltage gain of the proposed converter is enhanced through a reduction in the turn ratio of the coupled inductor, offering a significant benefit in minimizing the overall size of the converter. The reduction in the turns ratio of the coupled inductor results in lowered voltage stress on the semiconductor elements. Additionally, employing just one power switch in the converter simplifies control and reduces expenses. With its continuous input current, this converter is particularly well-suited for integration in photovoltaic systems. Simulation results conducted using PSCAD/EMTDC software validate the efficacy of the proposed power converter. Furthermore, the maximum power output of the photovoltaic module through an MPPT (Maximum Power Point Tracking) controller under varying irradiance levels is determined, and simulations are executed using PSCAD/EMTDC.

I. Introduction

Renewable energy technologies like solar (photovoltaic), fuel cells, and wind power are gaining popularity due to the increasing energy demands [1, 2]. This trend has spurred power industry professionals, organizations, and regulators to deepen their investigation of renewable energy sources [3, 4]. Solar PV panels primarily generate direct current (DC) with relatively low voltage levels. To efficiently elevate this voltage to higher levels, a high voltage conversion ratio converter is essential as an intermediary between the renewable energy source and the end user. A topology with high voltage gain, compact size, and low power losses is crucial for this task. DC-DC converters play a vital role in increasing voltage levels to match the load or DC bus requirements [5, 6]. Consequently, the development of high-voltage-gain converters has emerged as a significant solution to leverage renewable resources effectively [7, 8]. Various types of high-step-up DC-DC converters are being explored, broadly categorized into isolated and non-isolated classes for renewable energy applications [9, 10]. Non-isolated DC-DC converters offer advantages like smaller size, higher efficiency, and reduced production costs due to the absence of a transformer. In solar PV setups, DC-DC converters handle input voltage conversion from 12-60 V to a fixed output ranging from 24 V to 760 V. The demands for high-step-up DC-DC boost converters arise from the necessity for very high output voltages with limited input voltage ranges. It is critical for the DC-DC converters deployed in renewable energy systems to exhibit minimal input current ripple, as high ripple can reduce the lifespan of the solar panels and overall system efficiency. Hence, there arises a requirement for an appropriate input filter for the utilized DC-DC converter, and the filter used in these converters must be carefully selected to avoid an excessive increase in converter size and cost. Traditional DC-DC converters achieve high voltage gains through wide duty cycles,

leading to increased conduction losses and electromagnetic interference (EMI) issues [11, 12]. Furthermore, the voltage gain is limited in practice due to power losses in switches/diodes and the equivalent series resistance of capacitors and inductors. The enhancement of voltage conversion ratio through the use of switched capacitors and/or switched inductor units has been a subject of research [13, 14]. However, concerns related to electromagnetic interference (EMI) impose limitations on voltage boosting due to high duty cycle levels. Additionally, operational challenges arise at high step-up voltage ratios, leading to increased current stress levels that can result in component failures and reduced element lifetime [15, 16]. To address these issues, alternative traditional DC-DC converters such as forward, push-pull, and fly-back converters can be employed by adjusting the transformer's turns ratio. Various isolated converters have been presented to achieve high voltage conversion ratios, but their implementation comes with increased cost and volume due to the isolated configuration. To mitigate these challenges, non-isolated DC-DC converters offer a viable solution, presenting advantages such as lower cost and smaller volume. Various high-gain converters leveraging coupled inductors with minimal core loss can be employed. These converter topologies achieve high voltage gain by adjusting the duty cycle of the power switch and the turns ratio of the coupled inductor. An introduced non-isolated topology in [17] is suited for microgrid inverters; however, the high input current ripple associated with this design may diminish the operational lifespan of the input PV panels. Another high step-up structure presented in [18] involves a voltage multiplier cell (VMC) and coupled inductor, yet it also suffers from high input current ripple and a high component count, leading to reduced efficiency. Several DC-DC converters with high voltage gain benefits are presented in the literature. Despite these advancements, challenges persist in high step-up DC-DC converters, including issues such as high input current ripple, elevated voltage stress on semiconductor components, diode reverse recovery troubles, increased component count, and lower overall efficiency. In [19], an economical and effective converter known as the Z-source DC-DC converter was introduced. This converter implements the Z-source network using two inductors and two capacitors. The unique X-shaped interconnection of the inductors and capacitors in the Z-source network enables its integration with other converters and methodologies like the boost converter, switched-inductor, and switched capacitor [20-22]. However, due to its atypical non-grounded configuration, the basic Z-source converter is limited in its applications. To enhance the voltage gain, a combination of the switched-inductor and Z-source network was explored in [23], but this approach exhibited complexities, increased costs, and larger dimensions. Another prospect involved integrating a switched capacitor into a Z-source DC-DC converter [24], leading to a similarly intricate and expensive design that lacks common ground. Recent research efforts have aimed at addressing common grounding and reducing voltage stresses in such converters [25, 26]. For instance, a quasi-Z-source converter was introduced in [27] to mitigate issues like discontinuous input current and leakage current attributable to the absence of a common grounded connection between the output null and input negative terminal in the Z-source converter. The quasi-Z-source converter, akin to the Z-source counterpart, can be synergistically combined with techniques like switched capacitor and switched inductor to enhance characteristics such as voltage gain and voltage stress [28, 29]. Nevertheless, these combined converters necessitate additional components, escalating their complexity and cost. Moreover, the duty cycle of these converters is constrained by design limitations. In [30], a high-gain transformer-less converter employing a switched inductor, capacitor, and active network is presented. This configuration incorporates two switches, resulting in elevated conduction losses. Another converter described in [31] utilizes a coupled inductor and VMC, but the achieved voltage gain is modest. A high step-up structure with continuous input current is detailed in [32], utilizing a coupled inductor and voltage multiplier cell. Although a high voltage gain is achieved through increased turns ratio, this design suffers from high voltage stress on the main switch.

In this study, a single-switch transformer-less DC-DC converter with continuous input current is introduced. The proposed converter features a $CL^1C^2D^2$ network and offers several advantages, including high step-up gain with a low turn ratio of the coupled inductor, low voltage stress on the semiconductor devices, and a shared ground. The proposed converter features a straightforward design with a single power switch, devoid of any additional complexity in its topology. Simulation results conducted using PSCAD/EMTDC software are presented to verify the performance of the proposed converter. Additionally, the simulations involved the utilization of a photovoltaic module as an input source and the MPPT capability of the converter is confirmed.

II. Proposed DC-DC Converter

The configuration of the proposed converter is illustrated in Fig. 1. It comprises one power switch (S), three diodes (D_1, D_2, and D_3), one inductor (L), one coupled inductor (CL), four capacitors (C_1, C_2, C_3, and C_o). The proposed converter incorporates a conventional boost switching configuration with inductors L, switch S, diode D_1, and capacitor C_1 (resembling a conventional boost converter). Additionally, a $CL^1C^2D^2$ network is introduced, consisting of coupled inductor CL, capacitors C_2, C_3, diodes D_2, and D_3, situated between the conventional boost switching arrangement and the output capacitor C_o. The integration of the $CL^1C^2D^2$ network enhances the voltage gain of the proposed converter while alleviating the voltage stress on the semiconductor components.

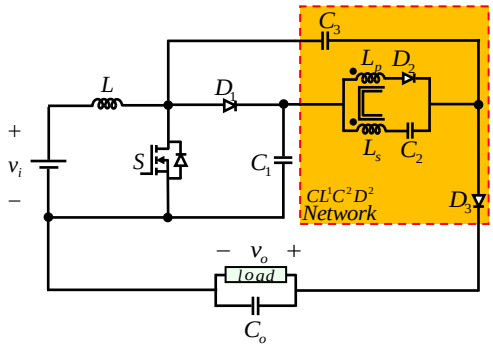

Fig. 1. The proposed converter.

The key waveforms for the proposed converter are depicted in Fig. 2. The proposed converters exhibit two distinct operational states: the shoot-through (ST) state, lasting DT_s, and the non-shoot-through (NST) state, lasting $(1\text{-}D)T_s$. In the proposed converter, the coupled inductor is conceptualized as a dual-headed transformer, depicted in Fig. 3. This transformer incorporates a magnetizing inductance (L_m) aligned in parallel with the primary winding. Therefore, the turns ratio of the coupled inductor is denoted as $n=N_S/N_P$. To express the conceptual performance of the proposed converter, several assumptions are considered in the analysis of the proposed converter: 1) Continuous conduction mode (CCM) is consistently maintained, 2) All components are assumed to be ideal, 3) The input DC source is constant, 4) The capacitors and inductors are sufficiently large, allowing for the application of the small ripple principle.

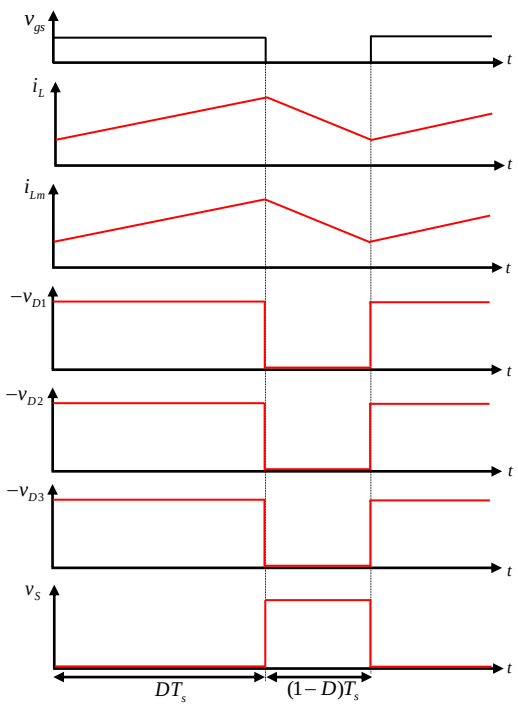

Fig. 2. Key waveforms of the proposed converter.

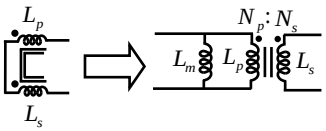

Fig. 3. Transformer modelling of the coupled inductor.

Shoot-through (ST) state: Fig. 4(a) demonstrates the corresponding circuitry depicting the ST state. During this state, the switch S is activated. The inductor L is charged in parallel with a voltage source via the S paths. Diodes D_1-D_3 are reverse-biased, preventing current flow. Furthermore, capacitors C_1 and C_2 are discharged while C_3 is being charged. Capacitor C_o delivers the necessary energy to the load and subsequently is discharged. By employing Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) in this operational state, the following equations can be formulated:

$$v_L = v_i \quad (1)$$
$$v_{Ls} = v_{C1} + v_{C2} - v_{C3} \quad (2)$$
$$v_{Co} = v_o \quad (3)$$
$$i_{Co} = -i_o \quad (4)$$
$$i_{C1} = i_{C2} = -i_{C3} = -i_{Ls} \quad (5)$$
$$i_{Lp} = i_{Lm} \quad (6)$$

Non-shoot-through (NST) state: This mode begins when the switch S is deactivated. Diodes D_1-D_3 transition to a forward bias state, enabling current conduction. The voltage across inductors L and magnetizing inductor L_m turns negative, leading to a linear reduction in their respective currents. Additionally, capacitors C_1, C_2, and C_o are charged, while C_3 is discharged during this state. Fig. 4(b) illustrates the equivalent circuitry representing this operational state. By applying KVL and KCL in this mode, the following equations can be expressed:

$$v_L = v_i - v_{C1} \quad (7)$$
$$v_{Lm} = -v_{C3} \quad (8)$$
$$v_{Ls} = v_{C2} - v_{C3} \quad (9)$$
$$v_{Co} = v_{C1} + v_{C3} \quad (10)$$
$$i_{C3} = i_{Lm} + i_{Ls} - i_{Lp} - i_{Co} - i_o \quad (11)$$
$$i_{C2} = -i_{Ls} \quad (12)$$
$$i_{C1} = i_L + i_{C3} + i_{Lp} - i_{Lm} - i_{Ls} \quad (13)$$

By applying the voltage balance principle to inductors L and L_m according to equations (1-3) and (7-10), the voltage across capacitors and the voltage gain of the proposed converter can be calculated as illustrated below:

$$v_{C1} = \frac{v_i}{1-D} \quad (14)$$
$$v_{C2} = \frac{(1-n)Dv_i}{n(1-D)} \quad (15)$$
$$v_{C3} = \frac{Dv_i}{n(1-D)} \quad (16)$$
$$v_o = v_{Co} = Gv_i = \frac{n+D}{n(1-D)}v_i \quad (17)$$

By utilizing the current balance principle for capacitors using equations (4-6) and (11-13), the mean current passing through the inductor and the magnetizing inductor can be evaluated as described subsequently:

$$i_L = \frac{n+D}{n(1-D)} i_o \tag{18}$$

$$i_{Lm} = i_o \tag{19}$$

where v_i, v_o and i_o are the input voltage, output voltage and output current, respectively. The voltage gain curves of the proposed converter are plotted in Fig. 5 for different coupled inductor's turn ratios. To demonstrate the impact of leakage inductance (L_k) on voltage gain, consideration is given to the coupling coefficient (k) as follows:

$$k = \frac{L_m}{L_k + L_m} \tag{20}$$

Fig. 6 illustrates the voltage gain of the proposed converter across varying coupling coefficients and duty cycles. It is observed that an increase in leakage inductance leads to a reduction in both coupling coefficient and voltage gain.

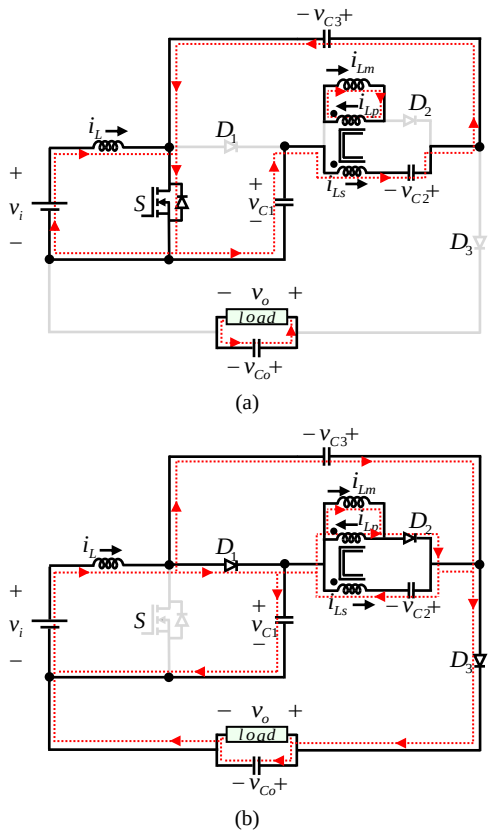

Fig. 4. Equivalent circuits of proposed converter. (a) ST. (b) NST.

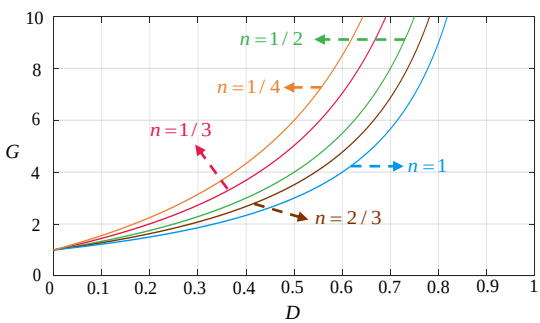

Fig. 5. Voltage gain versus duty cycle curves for four different coupled inductor's turn ratios.

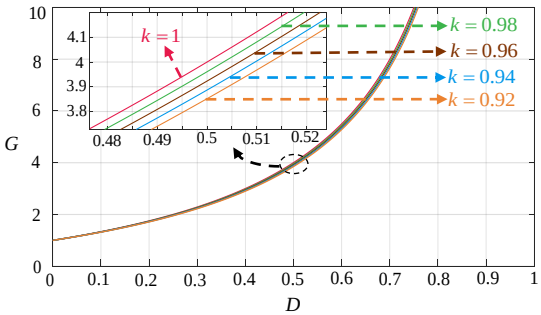

Fig. 6. Voltage gains versus duty cycle for different coupling coefficients (k) and n=0.5.

By applying KCL and the principle of current balance, it is possible to calculate the average currents of all capacitors during charging or discharging modes within a given time interval.

$$\begin{cases} i_{C1-charge} = i_{C2-charge} = \frac{Di_o}{n(1-D)} \\ i_{C1-discharge} = i_{C2-discharge} = -\frac{i_o}{n} \end{cases} \tag{21}$$

$$\begin{cases} i_{C3-charge} = \frac{i_o}{n} \\ i_{C3-discharge} = -\frac{Di_o}{n(1-D)} \end{cases} \tag{22}$$

$$\begin{cases} i_{Co-charge} = \frac{Di_o}{1-D} \\ i_{Co-discharge} = -i_o \end{cases} \tag{23}$$

Through the application of KVL to the equivalent circuit of the ST state, the voltages experienced across diodes D_1, D_2, and D_3 are determined using the following equations:

$$v_{D1} = v_{C1} = \frac{v_i}{1-D} \tag{24}$$

$$v_{D2} = v_{C1} - v_{C3} - v_{Lp} = \frac{(1-n)v_i}{n(1-D)} \tag{25}$$

$$v_{D3} = v_{C3} - v_o = \frac{v_i}{1-D} \tag{26}$$

Through the application of KVL to the equivalent circuit of the NST state, the voltage across the switch S is computed using the following equation:

$$v_S = v_{C1} = \frac{v_i}{1-D} \tag{27}$$

By utilizing KCL on the equivalent circuit during the ST state, the currents flowing through the switch S are determined using the ensuing equation:

$$i_S = i_L + i_{C3-charge} = \frac{(1+n)i_o}{n(1-D)} \tag{28}$$

Through the application of KCL to the equivalent circuit during the NST state, the currents flowing through diodes D_1, D_2, and D_3 are determined using the following equations:

$$i_{D1} = i_L + i_{C3-discharge} = \frac{i_o}{1-D} \tag{29}$$

$$i_{D2} = i_o + i_{Co-charge} + i_{C2-charge} + i_{C3-discharge} = \frac{i_o}{1-D} \tag{30}$$

$$i_{D3} = i_o + i_{Co-charge} = \frac{i_o}{1-D} \tag{31}$$

The root-mean-square (rms) values of the currents in the power switch, diodes and capacitors, as well as average currents of the switch and diodes play a crucial role in efficiency analysis, and they can be obtained as follows:

$$I_{S-rms} = \frac{\sqrt{D}(1+n)I_o}{n(1-D)} \quad (32)$$

$$I_{D1-rms} = I_{D2-rms} = I_{D3-rms} = \frac{I_o}{\sqrt{1-D}} \quad (33)$$

$$I_{C1-rms} = I_{C2-rms} = I_{C3-rms} = \sqrt{\frac{D}{1-D}}\frac{I_o}{n} \quad (34)$$

$$I_{Co-rms} = \sqrt{\frac{D}{1-D}}I_o \quad (35)$$

$$I_{S-ave} = \frac{D(1+n)I_o}{n(1-D)} \quad (36)$$

$$I_{D1-ave} = I_{D2-ave} = I_{D3-ave} = I_o \quad (37)$$

III. Parameter Design

The minimum value of the inductor is calculated by following equation:

$$L = \frac{|V_L|\Delta t}{\Delta I_L} \quad (38)$$

The voltage across the inductor during the $\Delta t = DT_S$ interval is represented by $|V_L|$. ΔI_L refers to the permissible percentage ripple inductor current, denoted as $\Delta I_L = x\%I_L$. By utilizing equations (1), (2), (18), (19) and (38), the minimum inductance values can be determined as such:

$$L \geq \frac{DV_i^2}{x\%f_sP_o} \quad (39)$$

$$L_m = \frac{D(n+D)V_i^2}{(1-D)x\%f_sP_o} \quad (40)$$

The minimum value of the capacitor is calculated by following equation:

$$C = \frac{|I_C|\Delta t}{\Delta V_C} \quad (41)$$

The current passing through the capacitor during the $\Delta t = DT_S$ interval is represented by $|I_C|$. ΔV_C denotes the voltage ripple across the capacitor, symbolized as $\Delta V_C = y\%V_C$. Thus, based on equations (4), (5), (14), (15), (16), (17) and (41), the necessary capacitances can be determined as follows:

$$C_1 \geq \frac{D(1-D)^2P_o}{(n+D)y\%f_sV_i^2} \quad (42)$$

$$C_2 \geq \frac{n(1-D)^2P_o}{(1-n)(n+D)y\%f_sV_i^2} \quad (43)$$

$$C_3 \geq \frac{n(1-D)^2P_o}{(n+D)y\%f_sV_i^2} \quad (44)$$

$$C_o \geq \frac{n^2D(1-D)^2P_o}{(n+D)^2y\%f_sV_i^2} \quad (45)$$

where, V_i, P_o, and f_s are the values of the input voltage, output power, and switching frequency, respectively. A methodological approach for the optimal selection of a magnetic core is outlined in [33]. The initial step involves the calculation of the geometrical constant (K_g) of the inductor and coupled inductor core utilized in the proposed converter, as defined by:

$$K_g = \frac{A_C^2W_A}{MLT} \geq \frac{\rho L^2I_{max}^2}{r_LK_uB_{max}^2} \quad (46)$$

Here, A_C represents the effective cross-sectional area of the core, MLT denotes the mean length turn, W_A represents the window area, ρ is the copper's resistivity, B_{max} stands for the maximum flux density of the ferrite core, and K_u signifies the window utilization factor. Substituting (18) and (39) into (46) allows for the determination of the geometrical constant (K_g) for the inductor L, as demonstrated below:

$$K_g = \frac{A_C^2W_A}{MLT} \geq \frac{\rho}{r_LK_uB_{max}^2\left(\frac{D(n+D)V_i^2I_o}{n(1-D)x\%f_sP_o}\right)^2} \quad (47)$$

Substituting (19) and (40) into (46) allows for the determination of the geometrical constant (K_g) for the coupled inductor L_m, as demonstrated below:

$$K_g = \frac{A_C^2W_A}{MLT} \geq \frac{\rho}{r_LK_uB_{max}^2\left(\frac{D(n+D)V_i^2I_o}{(1-D)x\%f_sP_o}\right)^2} \quad (48)$$

Upon selecting the most suitable core for the inductor and coupled inductor based on the A_C value, the calculations for the number of winding turns (n) and the air gap (l_g) are determined as outlined below:

$$n = \frac{LI_{max}}{A_CB_{max}} \quad (49)$$

$$l_g = \frac{\mu_0LI_{max}^2}{2B_{max}^2C} \quad (50)$$

where μ_0 is the permeability of air.

IV. Power Loss of Components

The primary components of losses in DC-DC converters are categorized into conduction loss and switching loss. Switching losses necessitate scrutiny in both diodes and power switches. The substantial current flow through components leads to significant conduction losses in the majority of cases. Therefore, an examination of the conduction losses in power switches, diodes, inductors, and capacitors is conducted for the converter.

Power switch losses: The conduction loss in the power switch can be expressed as:

$$P_{SC} = r_SI_{S-rms}^2 \quad (51)$$

Here, ($I_{S\text{-}rms}$) represents the rms current flowing through the power switch, while (r_S) denotes the resistance of the switch. By employing (32) and (51), the ultimate expression for the switch conduction loss can be formulated as:

$$P_{SC} = r_S\left(\frac{\sqrt{D}(1+n)I_o}{n(1-D)}\right)^2 \quad (52)$$

The turn-on and turn-off losses pertaining to a power switch can be described by a shared equation, exemplified by (53), as derived for the switch utilized in the proposed converter, as shown in (54).

$$P_{SS} = V_SI_{S-ave}(t_r + t_f)\frac{f_s}{2} \quad (53)$$

$$P_{SS} = \frac{D(1+n)(t_r+t_f)f_sP_o}{2n(1-D)^2} \quad (54)$$

Here, the P_{SS}, t_r, t_f, V_S, $I_{S\text{-}ave}$, and f_s represent the switching loss, turn-on delay time, turn-off delay time, switch voltage, average switch current, and switching frequency, respectively.

Diode power losses: The power loss in diodes can be categorized into conduction loss, forward voltage drop loss, and switching loss. Equation (55) details the forward voltage drop loss of a diode (P_{DF}), enabling the calculation of losses for the

diodes in the proposed converter. Equation (56) presents the total forward voltage drop loss of the diodes.

$$P_{DF} = V_F I_{D-ave} \quad (55)$$

$$P_{DF} = (V_{F1} + V_{F2} + V_{F3}) I_o \quad (56)$$

Where V_F and $I_{D\text{-}ave}$ denote the forward voltage drop of the diode and the average current through the diode, respectively. The next calculated loss for the diodes is conduction loss (P_{DC}). The total conduction loss of the diodes in the proposed converter is summarized as:

$$P_{DC} = (r_{D1} + r_{D2} + r_{D3}) \left(\frac{I_o}{\sqrt{1-D}}\right)^2 \quad (57)$$

The resistances r_{D1}, r_{D2}, and r_{D3} represent the resistances of the diodes in the proposed converter. The final aspect of diode losses is the switching loss (P_{DS}), for which a standard equation is presented as (58). Equation (59) is formulated specifically for the switching loss pertaining to the diodes in the proposed converter.

$$P_{DS} = V_D I_{D-ave} t_{rr} \frac{f_s}{2} \quad (58)$$

$$P_{DS} = \left(\frac{(1-n)}{n(1-D)} + \frac{2}{(1-D)}\right) P_o t_{rr} \frac{f_s}{2} \quad (59)$$

The parameters t_{rr}, V_D, and $I_{D\text{-}ave}$ denote the reverse recovery time, diode voltage, and average diode current, respectively.

Inductors conduction loss: The conduction loss for the inductors (P_{LC}) is computed based on equation (60) and is expressed as equation (61).

$$P_{LC} = r_L I_{L-rms}^2 \quad (60)$$

$$P_{LC} = r_L \left(\frac{n+D}{n(1-D)} i_o\right)^2 + r_{Lm} I_o^2 \quad (61)$$

Capacitors conduction loss: The conduction loss in the proposed converter stems from the resistance in capacitors. The converter in question incorporates four capacitors, the total conduction loss of which amounts to:

$$P_{CC} = (r_{C1} + r_{C2} + r_{C3}) \frac{D}{1-D} \left(\frac{I_o}{n}\right)^2 + r_{Co} \frac{D}{1-D} I_o^2 \quad (62)$$

The conduction loss of the capacitors and the resistance of the capacitors are denoted as P_{CC} and r_C, respectively. Consequently, the efficiency of the proposed converter can be ascertained:

$$\eta = \frac{P_o}{P_o + P_{Loss}} \quad (63)$$

To analyze the impact of parasitic elements in both passive and active components on the voltage gain of the proposed converter, the model of the converter was modified to incorporate these elements. Fig. 7 depicts the circuit of the proposed converter with the integrated parasitic elements. This non-ideal converter model accounts for several parasitic elements, including the series resistances of the inductors ($r_L = r_{Lm} \approx r_L$), the equivalent series resistances of the capacitors ($r_{C1} = r_{C2} = r_{C3} = r_{Co} \approx r_C$), the on resistance of the power switch (r_S), the forward resistances of the diodes ($r_{D1} = r_{D2} = r_{D3} \approx r_D$), and their corresponding forward voltages ($V_{F1} = V_{F2} = V_{F3} \approx V_F$). Considering these parasitic elements, a new equation was derived to characterize the static voltage gain of the proposed converter (G') in equation (64).

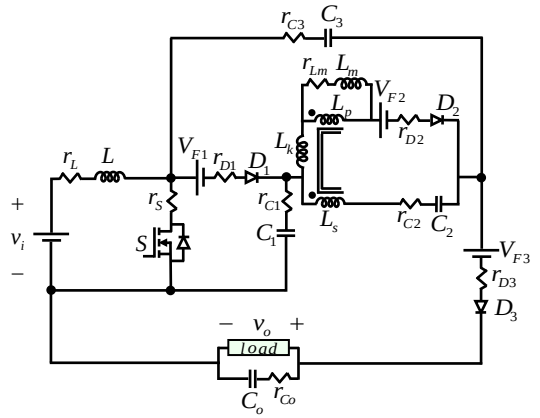

Fig. 7. The proposed converter with the parasitic elements.

V. Comparative Analysis

Table 1 presents a comparison of the characteristics of the proposed converter with similar converters. The results from Table 1 are illustrated in Figs. 8(a)-8(c). Fig. 8(a) displays the variation of voltage gain versus the duty cycle. It is evident that the proposed converter exhibits a higher voltage gain for n=0.5 compared to others with the same duty cycle except [28, 29]. However, the converters [28, 29] have a duty cycle limitation and suffer from high voltage stress on their semiconductors. For lower duty cycles, the converter described in [17, 31, 32] shows the highest voltage gain, although it may not be suitable for high-gain applications. Fig. 8(b) portrays the variation of normalized voltage stress on the main switch with respect to the duty cycle. The proposed converter demonstrates lower voltage stress on switch S compared to other converters. According to Fig. 8(c), the plot of normalized voltage stress across diodes for various duty cycles with n=0.5 reveals that the proposed configuration's stress is lower than of the most other converters except [2, 31]. Importantly, the proposed converter achieves higher voltage gain with lower voltage stress on the power switch compared to [2, 31]. In contrast to the converters discussed in references [9, 15, 28], the proposed converter introduces a common grounded feature, crucial for electrical systems, particularly in photovoltaic applications. This characteristic plays a vital role in mitigating leakage currents, a prevalent concern in PV-based converters. In contrast to the converters in references [15, 17, 28, 31], the proposed converter ensures continuous input current and eliminates the need for bulky input filters. Unlike the ZS and QZS converters described in references [27-29] with a restricted duty cycle range of 0 to 0.5, the proposed converter overcomes duty cycle limitations, enabling a duty cycle variation from 0 to 1. By comparing the proposed converter to similar converters, it becomes apparent that the proposed topology offers higher voltage gain with reduced stress on the semiconductors. Consequently, this design could be effectively utilized in renewable energy systems such as PV applications with low implementation costs.

TABLE 1: COMPARISON OF THE PROPOSED CONVERTER WITH COMPARABLE CONVERTERS

Ref.	S[1]/D[2]/C[3]/L[4]/CL[5]	V_o/V_i	V_S/V_o	V_D/V_o	Common ground	Continuous input current	Duty cycle limitation
[2]	1/2/3/1/1	$\frac{1+nD}{1-D}$	$\frac{1}{1+nD}$	$\frac{n}{1+nD}$	Yes	Yes	No
[9]	1/4/4/3/1	$\frac{n}{1-D}$	$\frac{1}{n}$	1	No	Yes	No
[11]	2/2/4/1/1	$\frac{n}{1-D}$	$\frac{1}{n}$	1	Yes	Yes	No
[15]	2/5/4/-/1	$\frac{n(2-D)}{1-D}$	$\frac{1}{n(2-D)}$	$\frac{1}{2-D}$	No	No	No
[17]	1/3/3/-/1	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	1	Yes	No	No
[27]	1/2/3/2/-	$\frac{1}{1-2D}$	1	1	Yes	Yes	Yes
[28]	1/3/5/3/-	$\frac{1+D}{1-2D}$	$\frac{1}{1+D}$	$\frac{1}{1+D}$	No	No	Yes
[29]	1/5/3/3/-	$\frac{1+D}{1-2D-D^2}$	1	1	Yes	Yes	Yes
[31]	1/3/3/-/1	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{n}{1+n}$	Yes	No	No
[32]	1/3/4/1/1	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{1+n-D}{1+n}$	Yes	Yes	No
Proposed	1/3/4/1/1	$\frac{n+D}{n(1-D)}$	$\frac{n}{n+D}$	$\frac{n}{n+D}$	Yes	Yes	No

Number of 1. Switches, 2. Diodes, 3. Capacitors, 4. Inductors, 5. Coupled inductors

$$G' = \frac{(n+D)(1-D)RnV_o}{(Rn^2(1-D)^2V_o+r_sD(1+n)^2(1-D)V_o+3r_Dn^2V_o(1-D)+r_L(n+D)^2V_o+r_Ln^2(1-D)^2V_o+3r_CDV_o(1-D)+r_CD(1-D)n^2V_o+3V_FRn^2(1-D)^2)} \quad (64)$$

VI. Simulation Results

To verify the efficacy and confirm the reliability of the proposed converter, simulation outcomes are showcased using PSCAD/EMTDC software. The simulation parameters utilized are detailed in Table 2.

TABLE 2: PARAMETERS USED IN THE SIMULATION

Parameters and Values						
V_i	f_S	D	n	C_1-C_3, C_o	L, L_m	load
$40\,V$	50KHZ	0.3	0.5	$220\mu F$	$400\mu H$	15Ω

The results of the simulation are presented in Fig. 9. In Fig. 9(a), the output voltage is around $87.24\,V$, which agrees with the calculated value (V_o=91.4 V) for an input voltage (V_i) of 40 $V$and utilizing the voltage gain equation (17) with a duty cycle of 0.3. This alignment between the simulation and theoretical outcomes confirms the precision of the voltage gain. Fig. 9(b) displays the current waveform, showing an output current of 5.82A. The voltage and current stresses on the inductors are illustrated in Fig. 9(c)-9(f). The average current passing through inductors L and L_m is determined to be $13.34A$ and $5.73A$, respectively, as depicted in Fig. 9(d) and Fig. 9(f), which corresponds well with the theoretical predictions in equations (18)-(19). The waveforms of voltage stress on the capacitors, switches, and diodes are demonstrated in Fig. 9(g)-9(m). The calculated voltage stress values on the capacitors using equations (14)-(16), and on the switches and diodes using equations (24)-(27), closely correspond with the simulation results, as shown in Fig. 9(g) to Fig. 9(m).

VII. MPPT Simulation Results

In this section, the performance of the proposed converter under Maximum Power Point Tracking (MPPT) of a Photovoltaic (PV) system is evaluated using results obtained from PSCAD/EMTDC simulations. The setup of the proposed converter within a PV system is depicted in Fig. 10. A silicon module LG400N2W-A5 serves as the PV source, and its characteristics are detailed in Table 3 based on the manufacturer's datasheet. The P-V (power versus voltage) characteristic curves for radiations of $1000\,W/m^2$ and $800\,W/m^2$ at a temperature of T=298K are displayed in Figs. 11(a) and 11(b), respectively. As the change in radiation has a greater impact on the MPP compared to temperature variation, this study maintains a constant temperature and examines MPPT under various radiation conditions. Fig. 12 portrays the results obtained for the output power of the PV (P_{PV}), the output voltage of the PV (V_{PV}), the output voltage of the load (V_o), and radiation (G) during the extraction of maximum power from the PV with the proposed converter under step changes in radiation

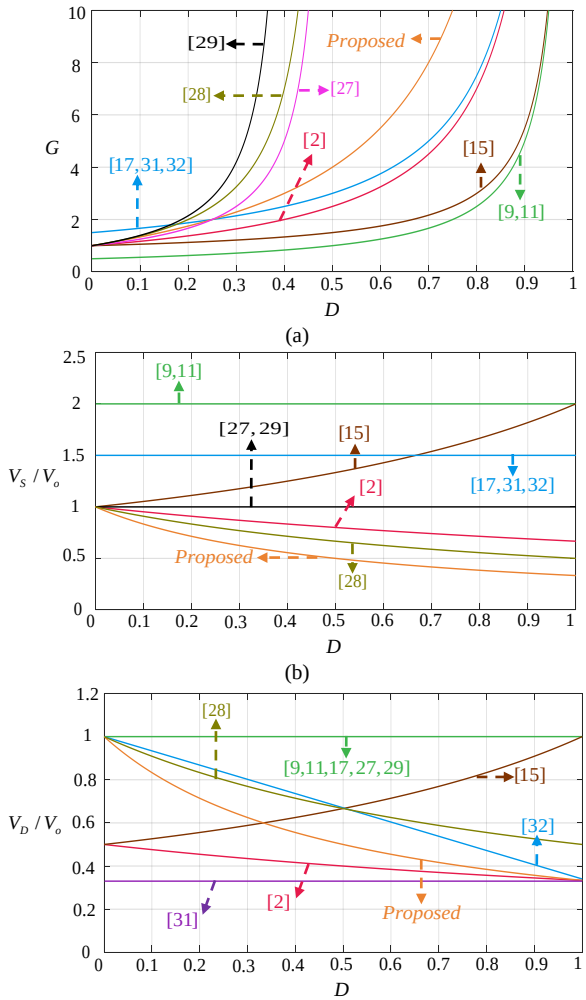

Fig. 8. Comparison results of the proposed converter and other converters. (a) voltage gain. (b) voltage stress on the switch. (c) voltage stress on diodes.

from $1000\,W/m^2$ to $800\,W/m^2$. The MPPT capability of the proposed converter is validated based on the P-V characteristics in Fig. 11 and the output power of the PV source in Fig. 12(a).

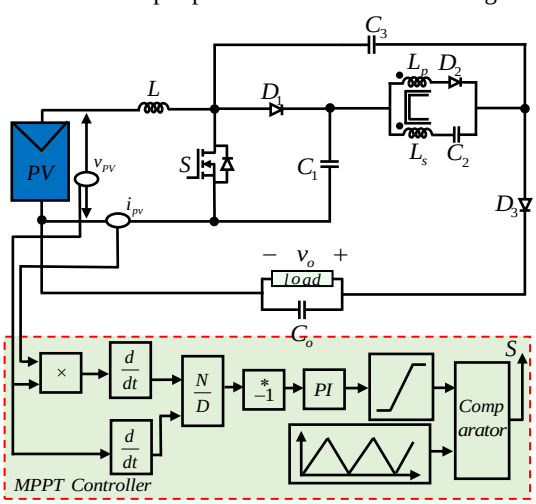

Fig. 10. Proposed converter and MPPT controller.

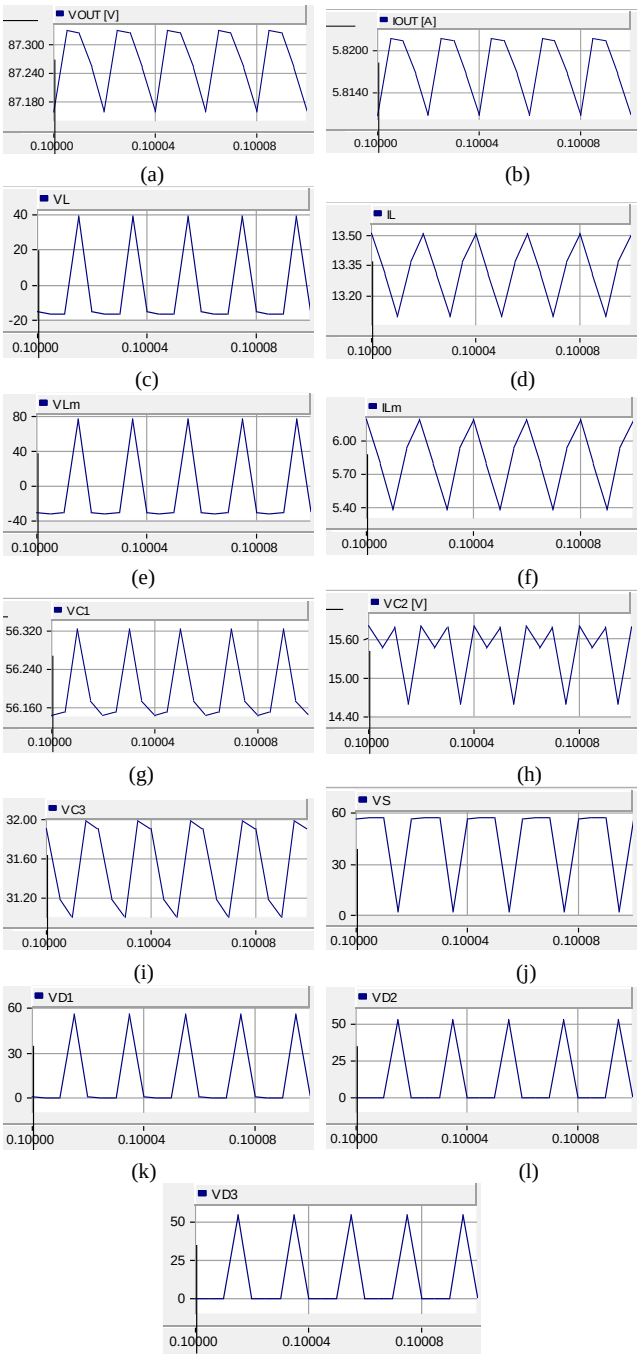

Fig. 9. Simulation results of the proposed converter.

TABLE 3: MONOCRYSTALLINE / N-TYPE MODULE PARAMETERS (LG400N2W-A5) PROVIDED BY THE MANUFACTURER FOR THE STANDARD CONDITION

Parameters and Values					
P_{MPP}	I_{sc}	V_{oc}	V_{mpp}	I_{mpp}	N_s
$400\,W$	$10.47A$	$49.3V$	$40.6V$	$9.86A$	72

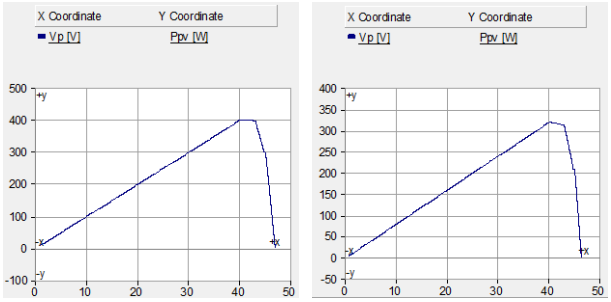

Fig. 11. Power versus voltage characteristic curves for radiations 1000 W/m^2 and 800 W/m^2 at temperature T=298 K. (a) 1000 W/m^2. (b) 800 W/m^2.

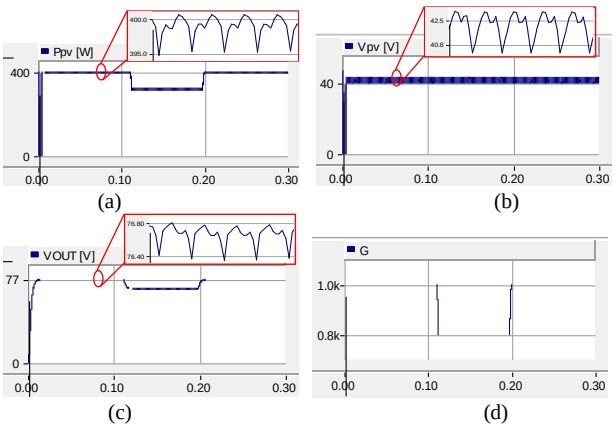

Fig. 12. MPPT simulation results for the proposed converter under step change of radiation from 1000 W/m^2 to 800 W/m^2 and 800 W/m^2 to 1000 W/m^2. (a) P_{PV}. (b) V_{PV}. (d) V_o. (a) irradiance (G).

VIII. Conclusion

In this research article, a single switch transformer-less DC-DC converter with continuous input current is introduced. This converter utilizes only a single power MOSFET, leading to a reduction in converter costs. Additionally, it features semiconductors with low blocking voltage, offering added advantages. A high voltage gain can be attained by decreasing the turn ratio of the coupled inductor, obviating the necessity for a high turn ratio to achieve a high voltage gain. Moreover, being transformer-less, the proposed converter circumvents associated drawbacks. A simple pulse width modulation technique is implemented for switch control. The converter incorporates MPPT control to optimize photovoltaic system power extraction. The theoretical analysis of the converter covers its operational modes, and the accuracy of the calculated outcomes is confirmed by comparing them with results from PSCAD/EMTDC software simulations.

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